Hybrid TLB Coalescing: Improving TLB Translation Coverage under Diverse Fragmented Memory Allocations

Chang Hyun Park, *Taekyung Heo, Jungi Jeong, and Jaehyuk Huh*

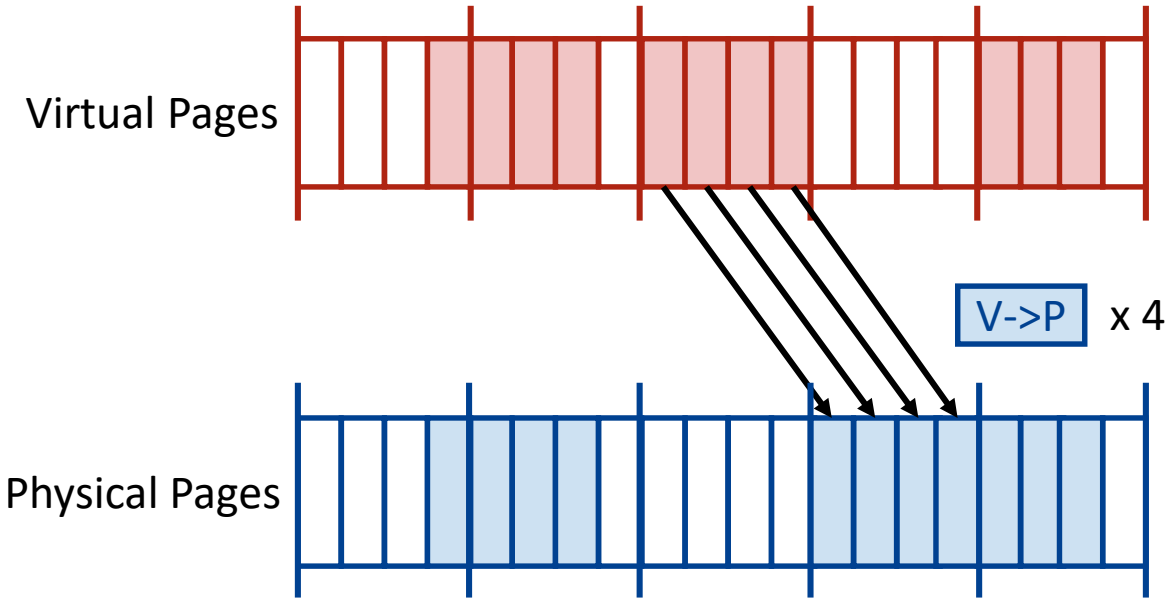
KAIST School of Computing

Introduction

- Virtual memory provides rich features
  - Requires an address translation
- Workloads have grown in size pressuring TLB
- Contiguous memory allocations to the rescue!

Past Proposals: Large pages

- Large pages represent larger mappings (2MB)
  - Strict alignment required
  - Exact size match required



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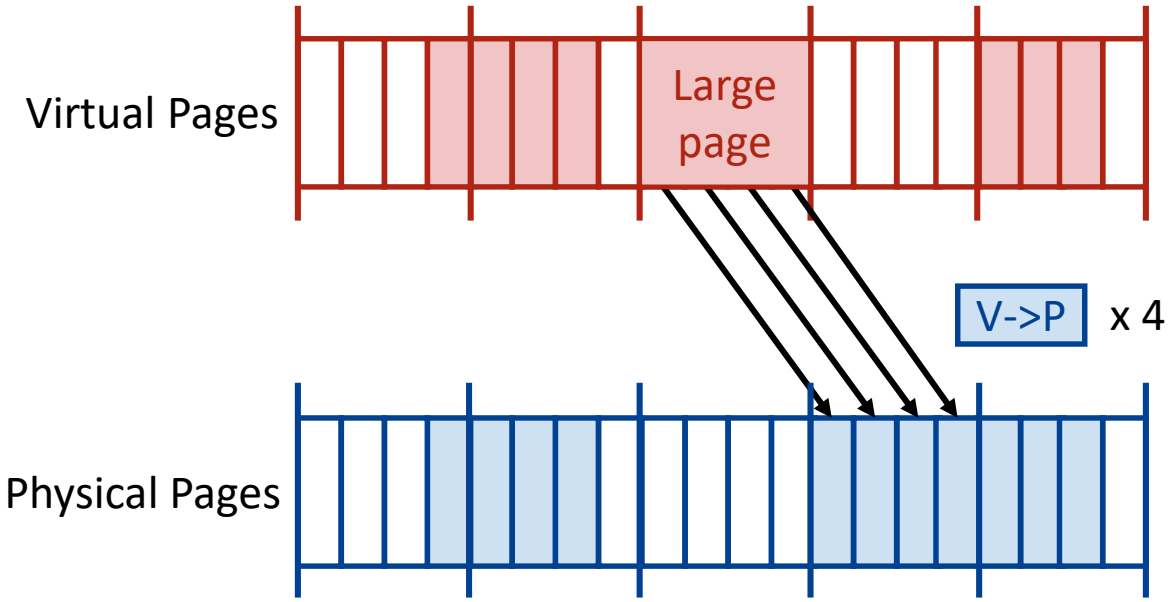

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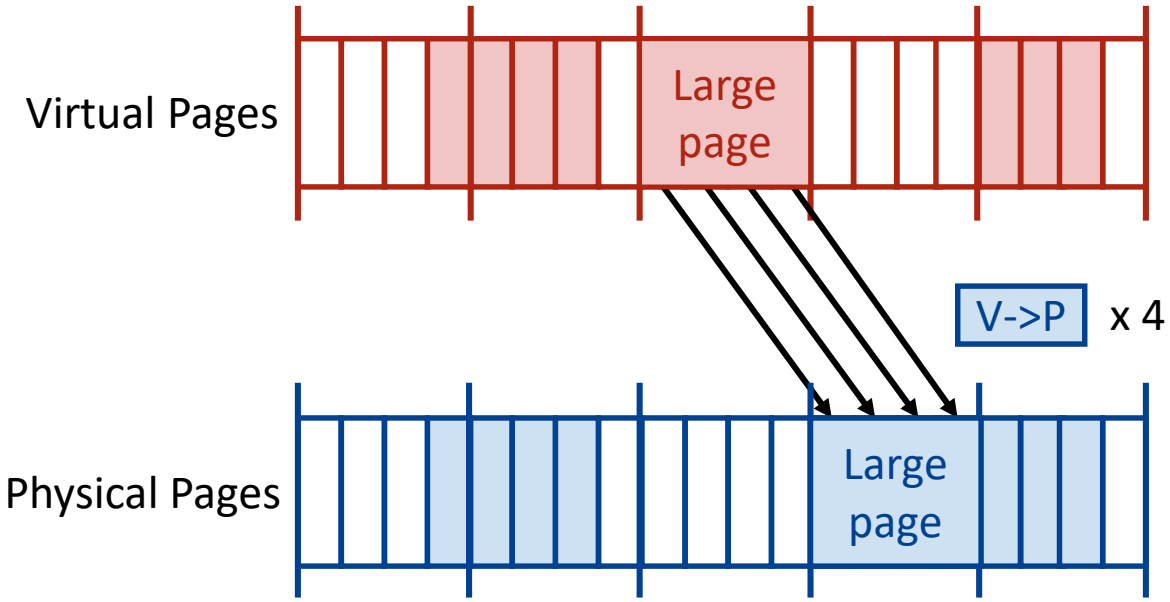

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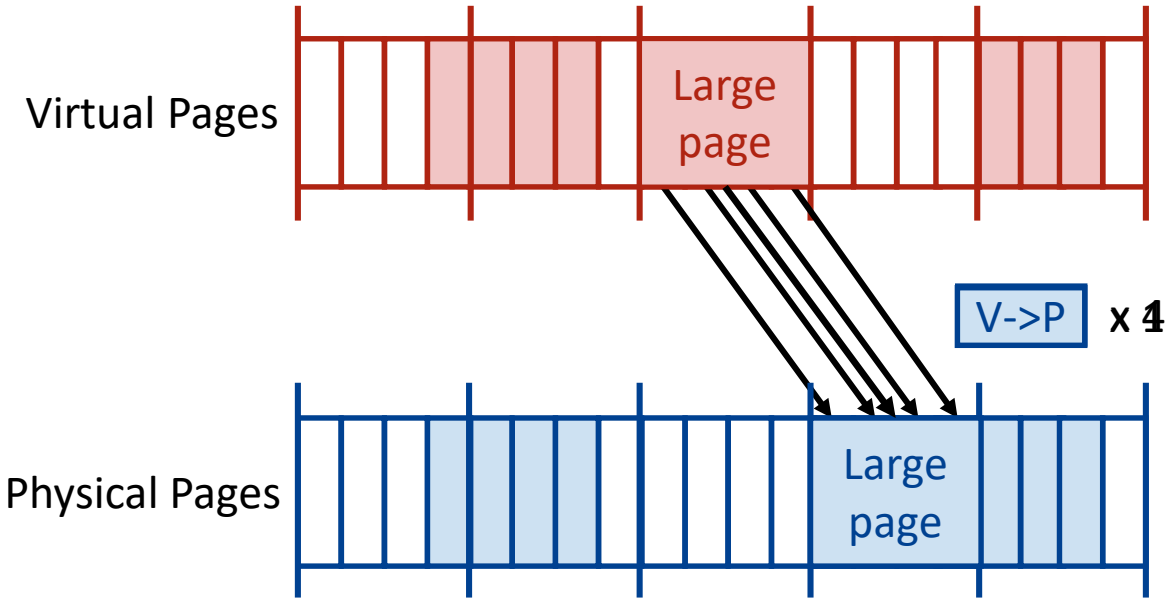

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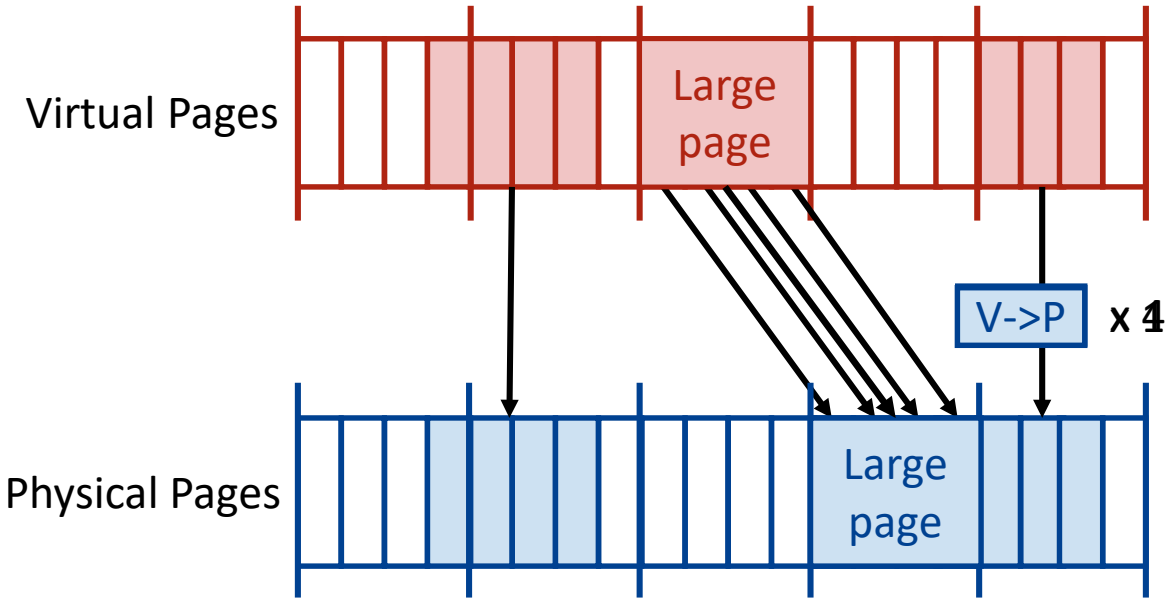

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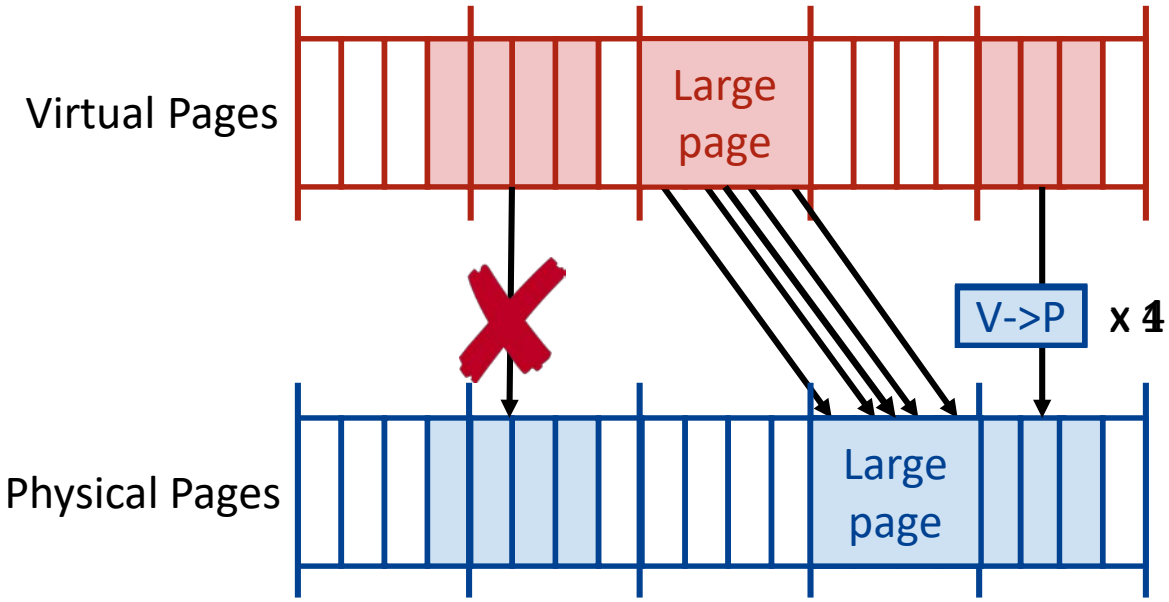

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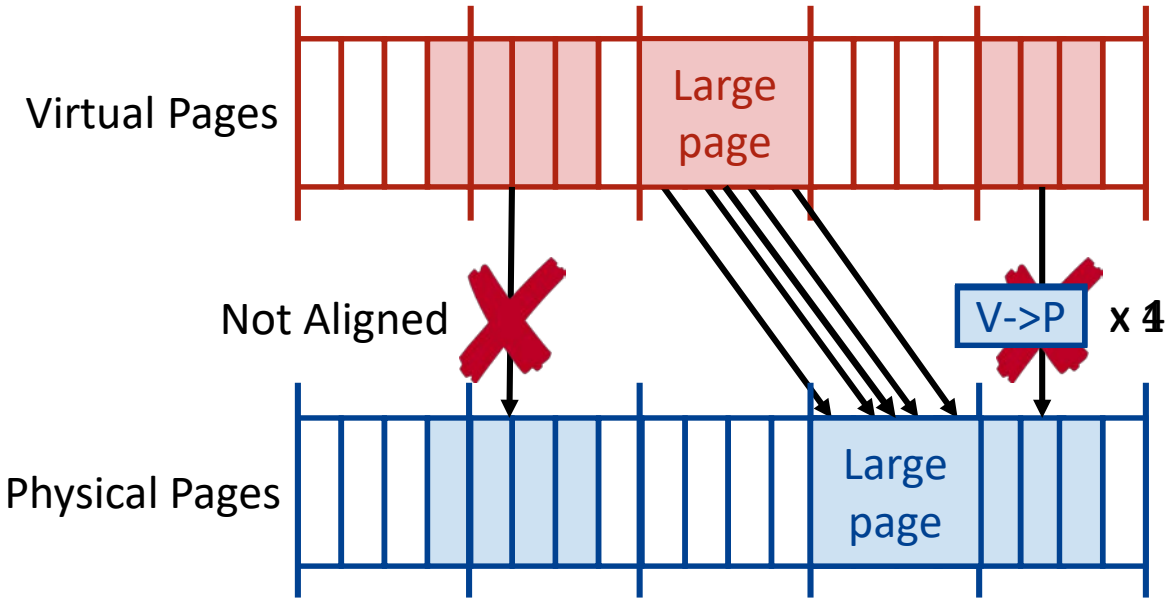

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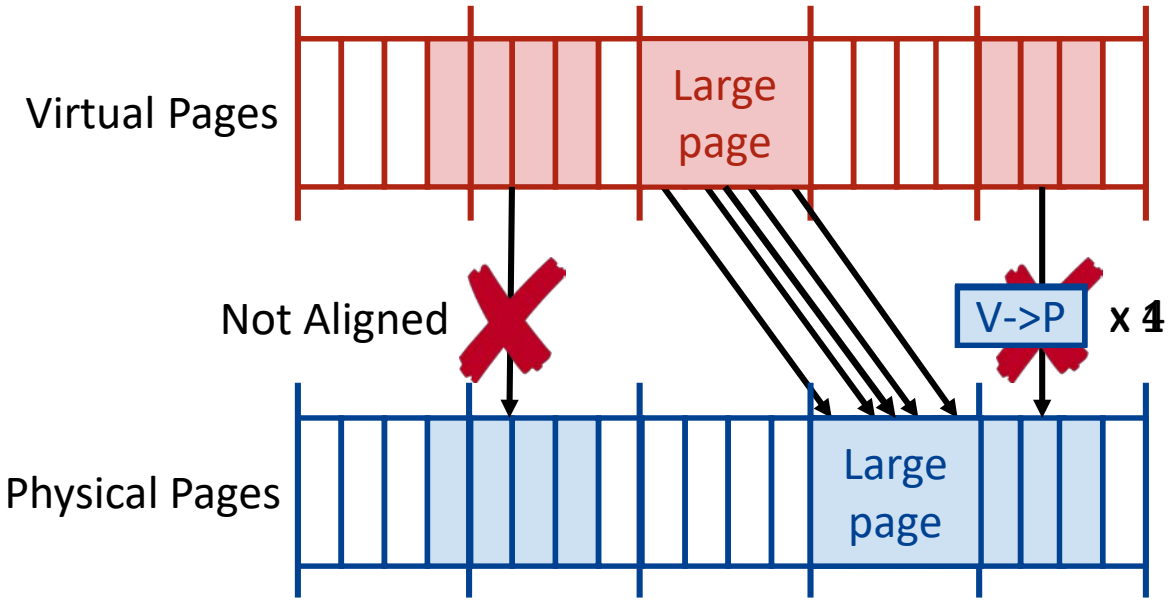

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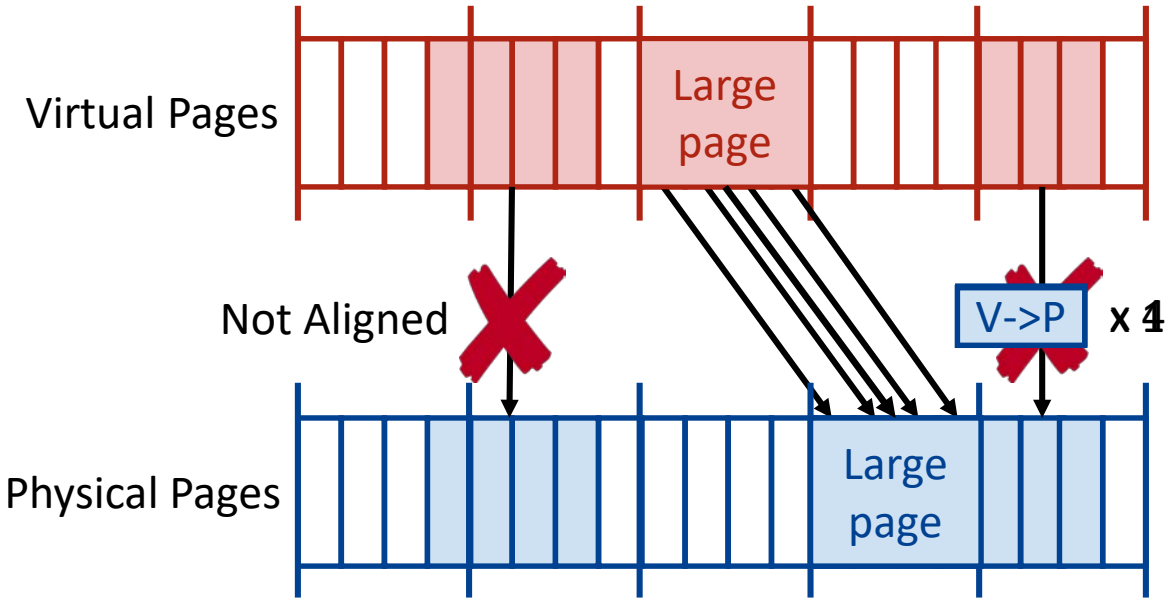

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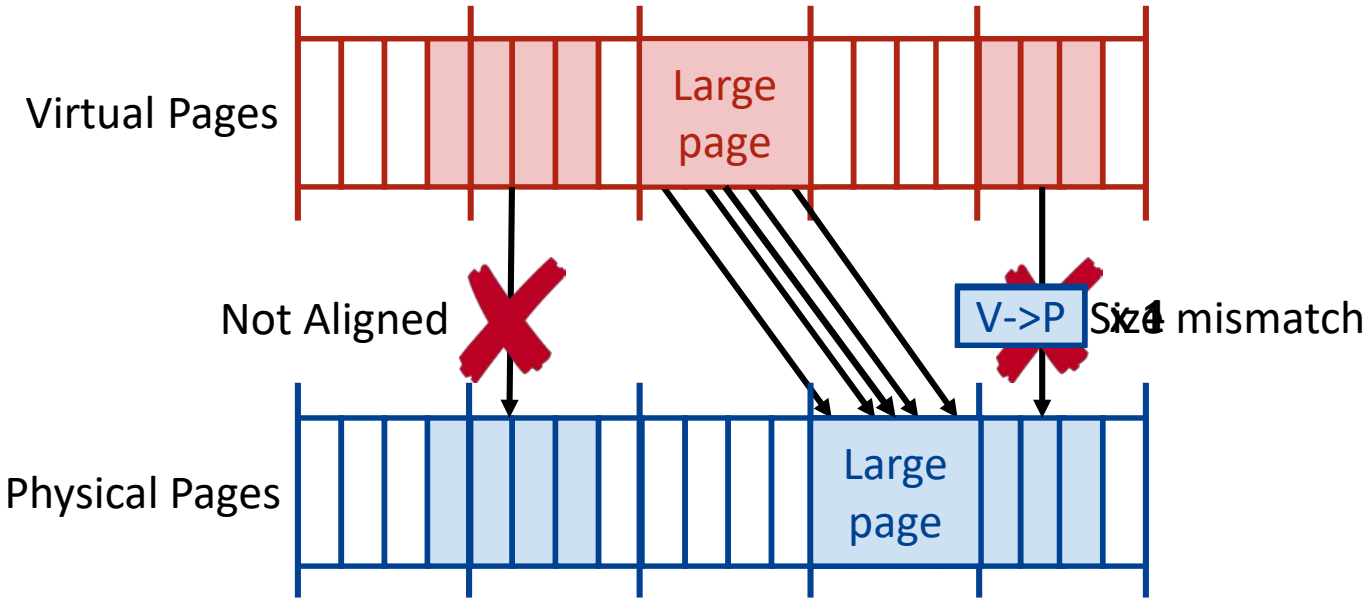

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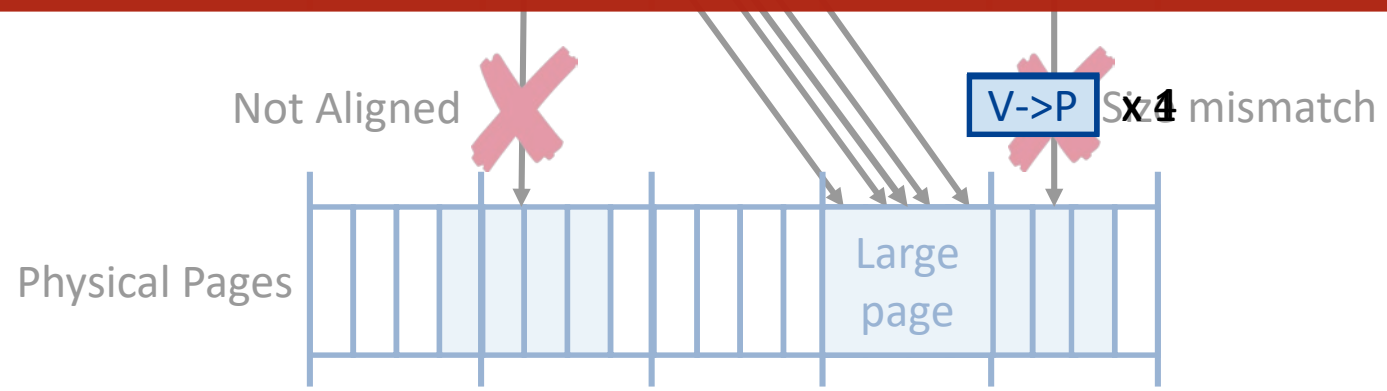
Efficient when large pages provided by OS



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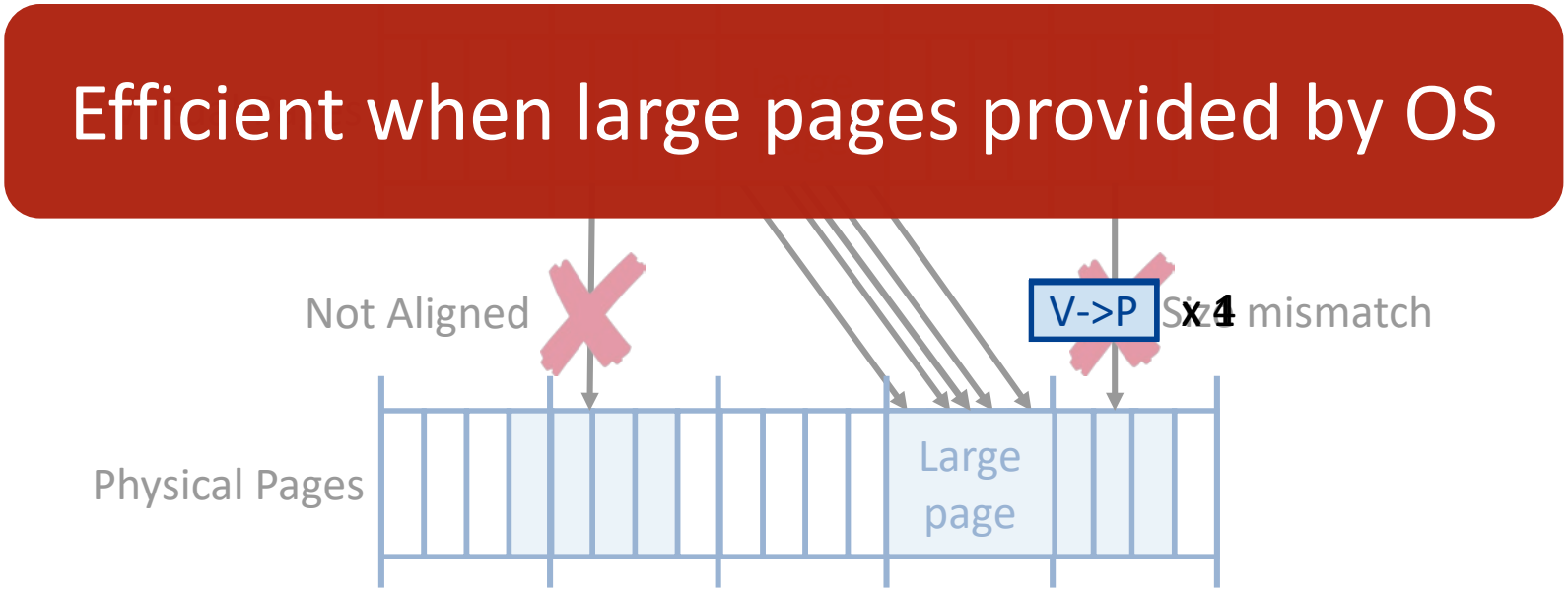

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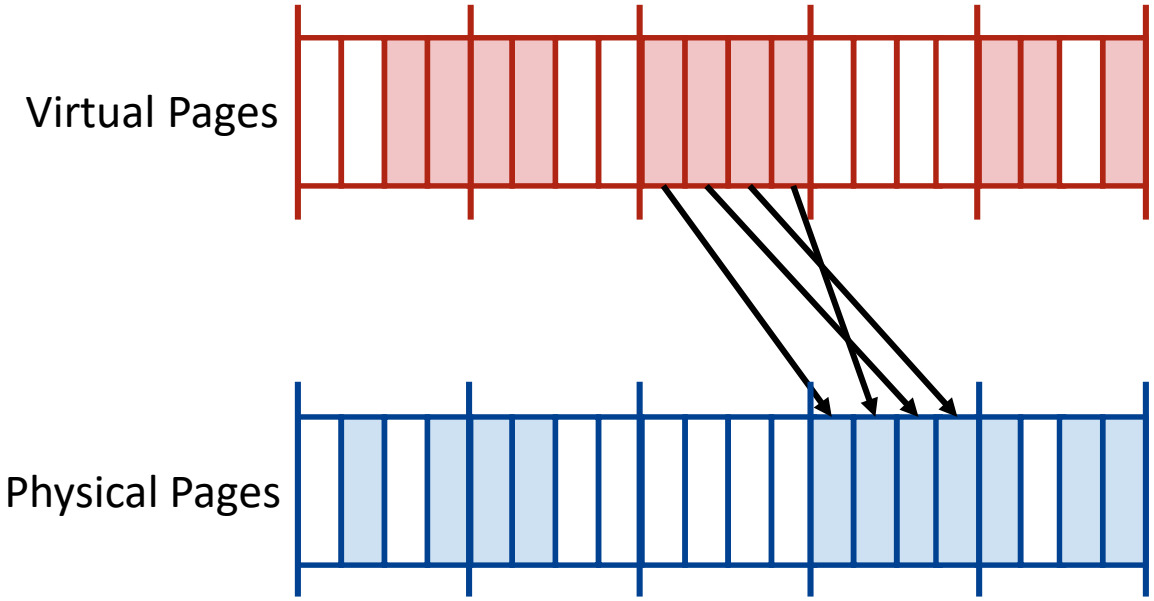

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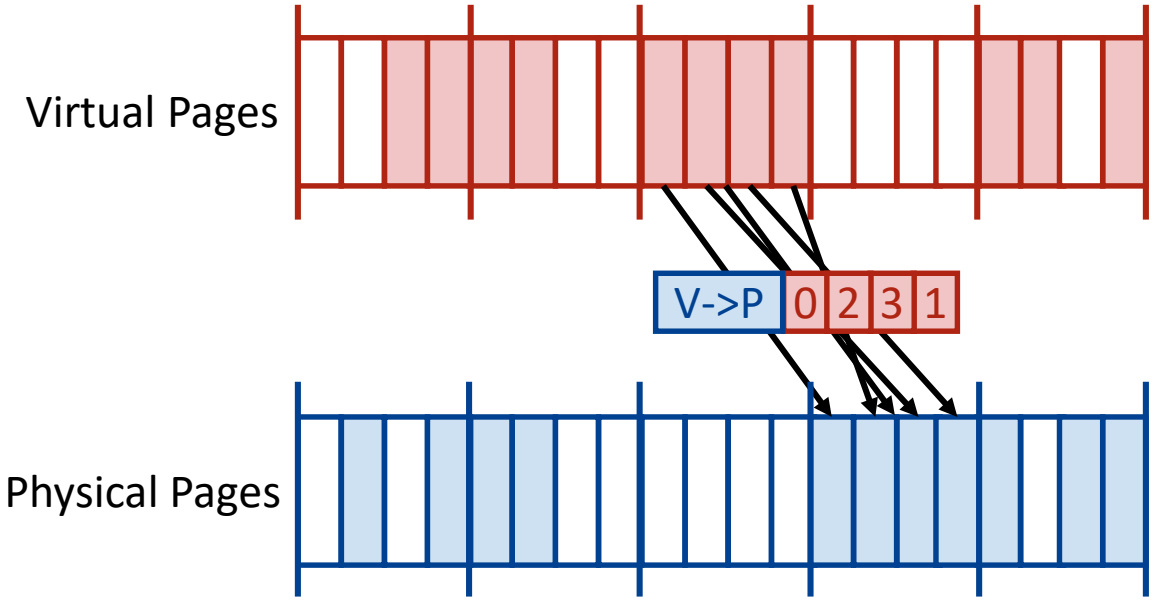

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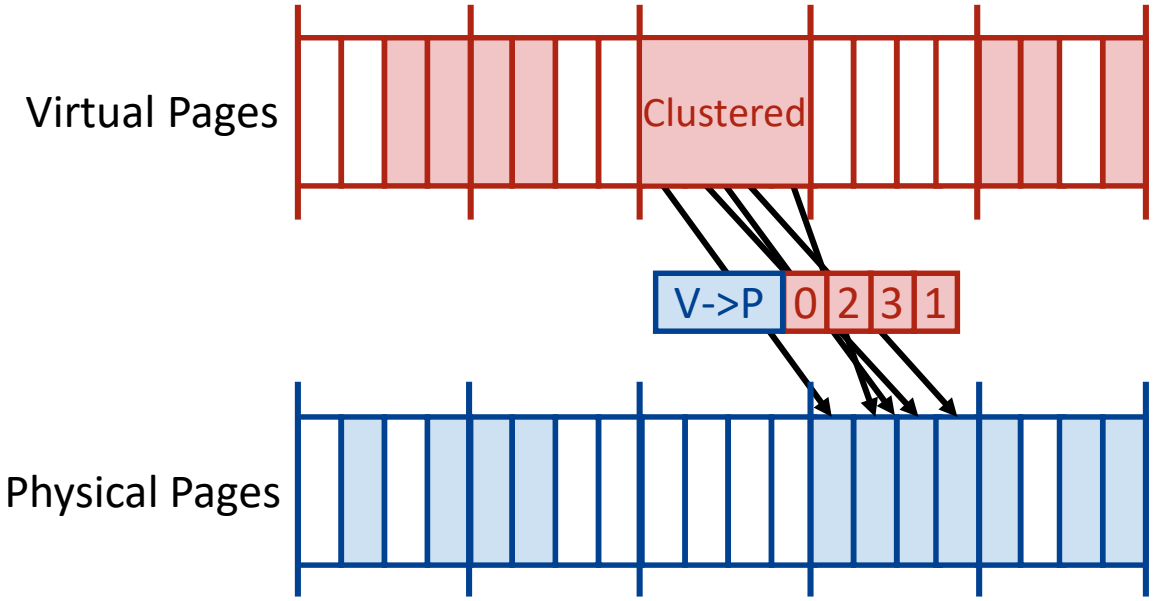

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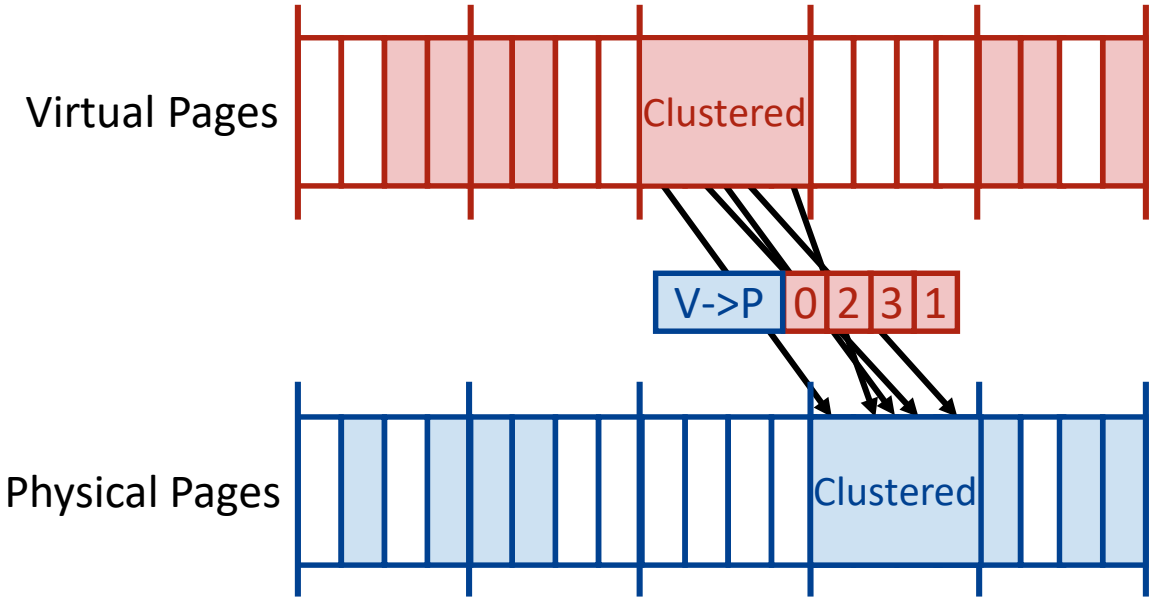

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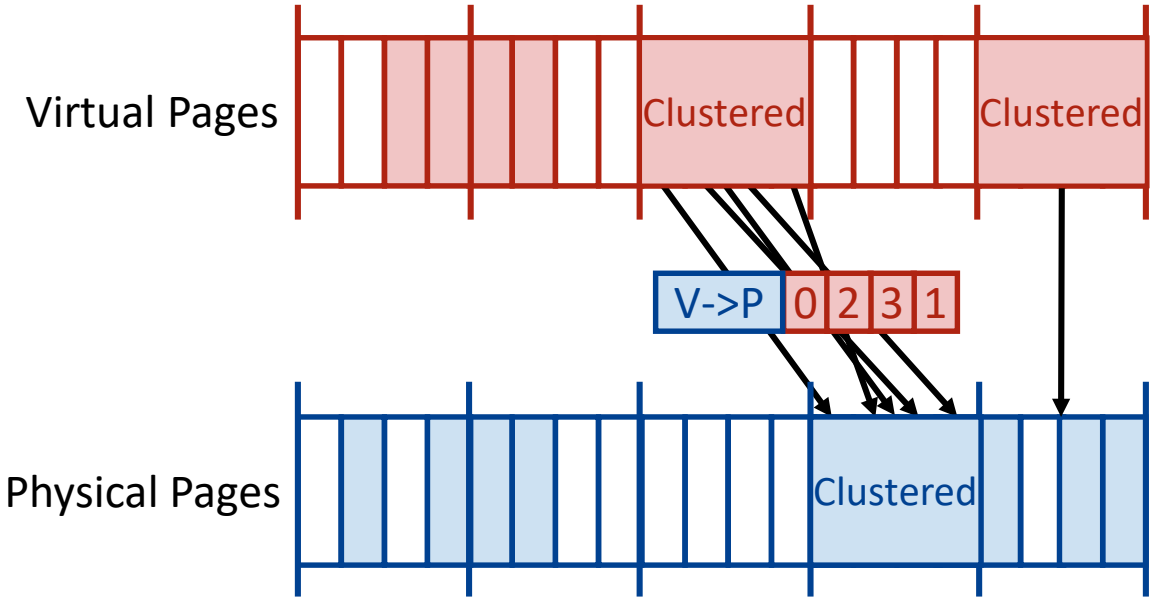

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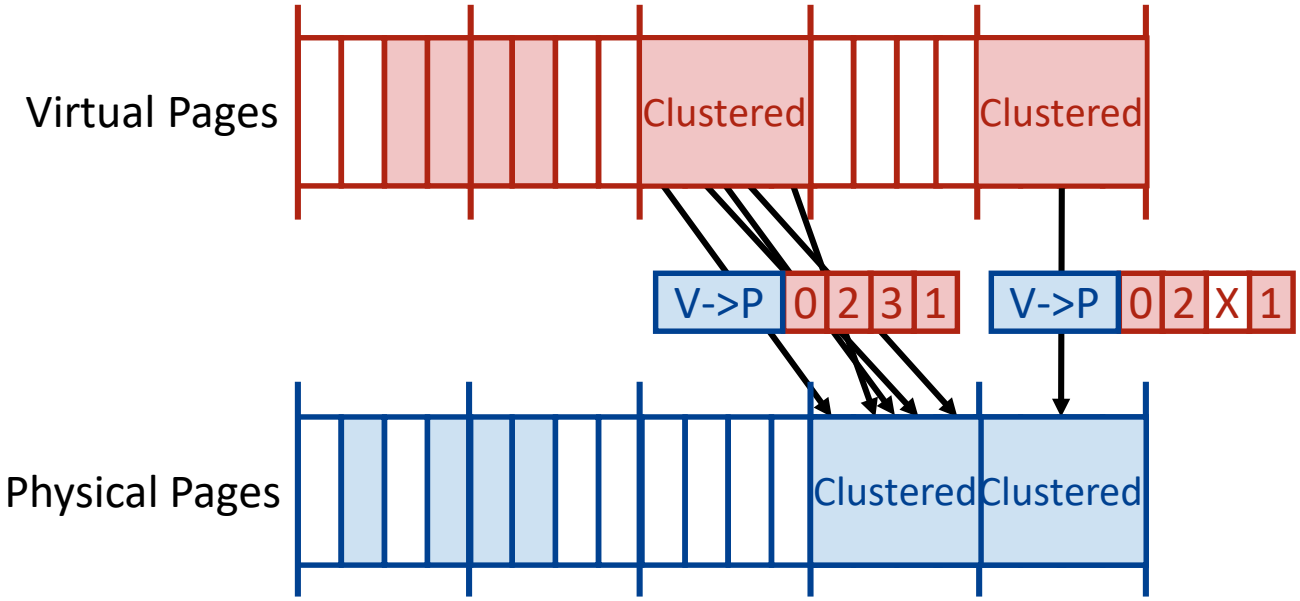

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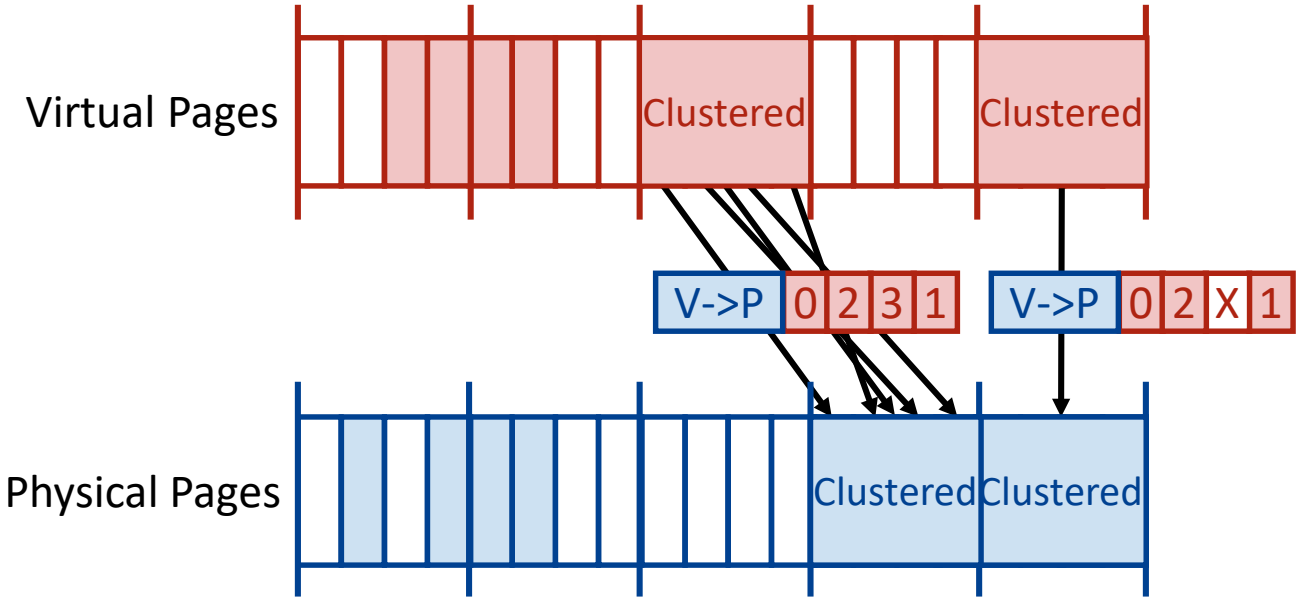

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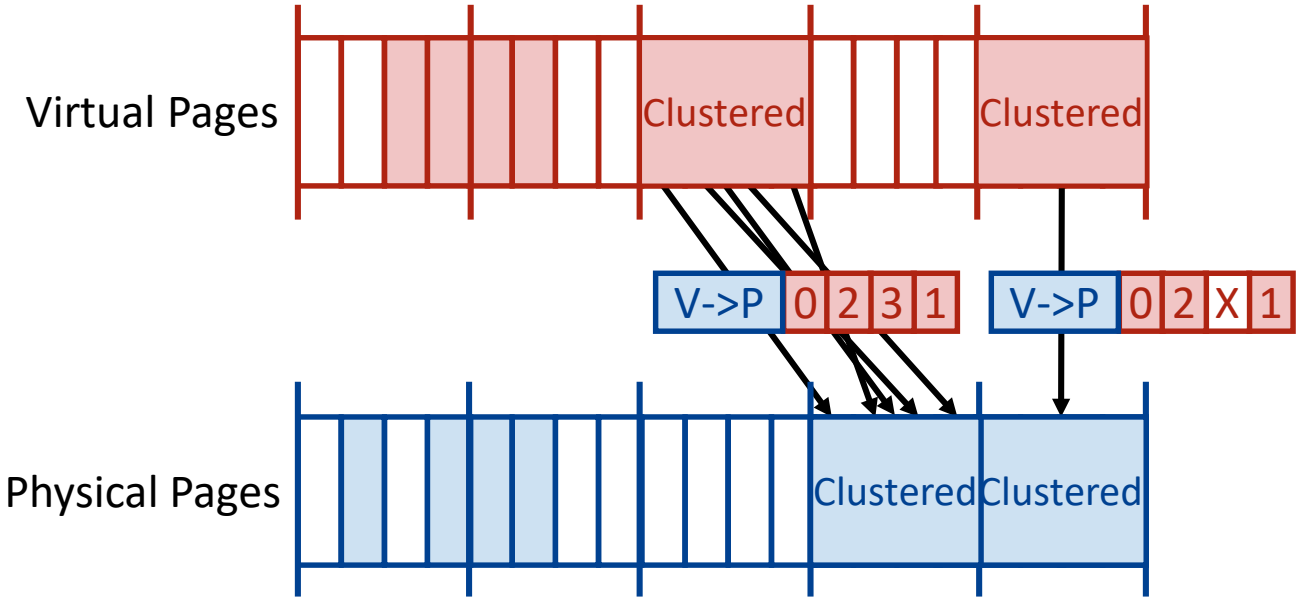

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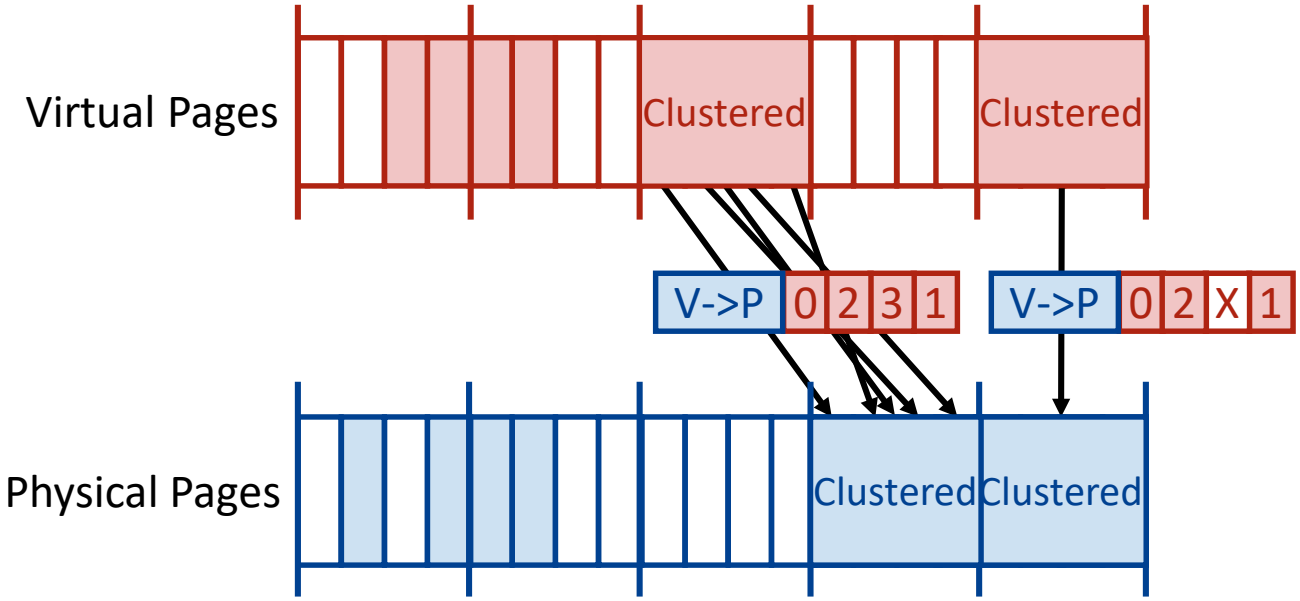

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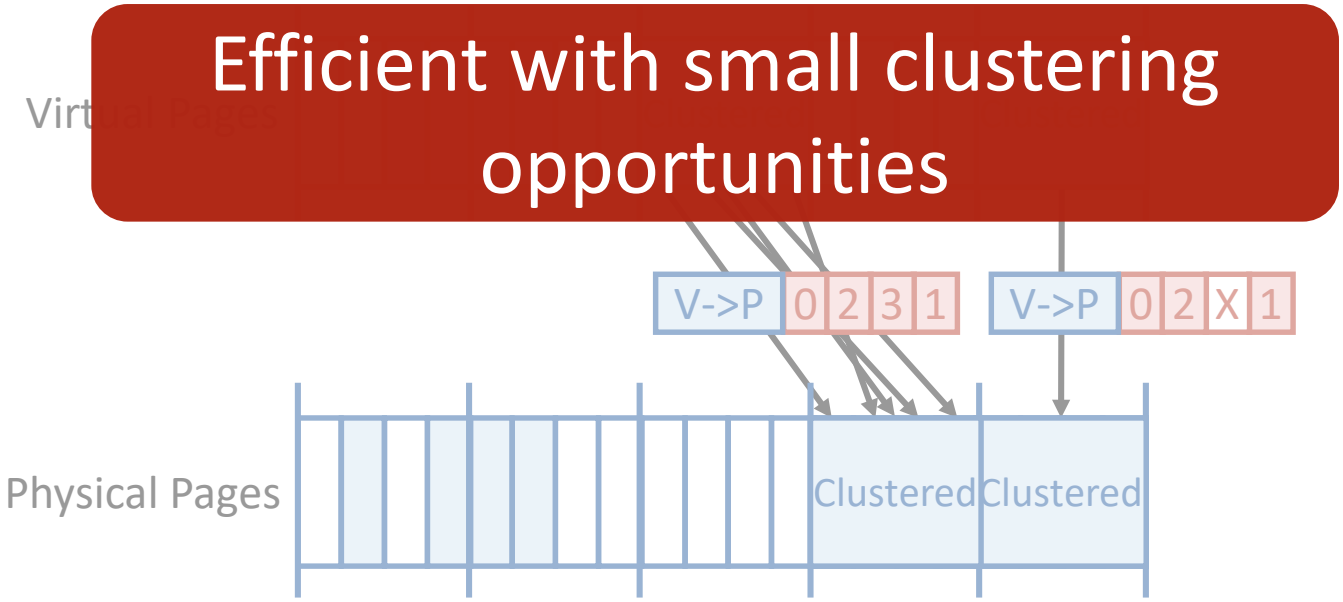

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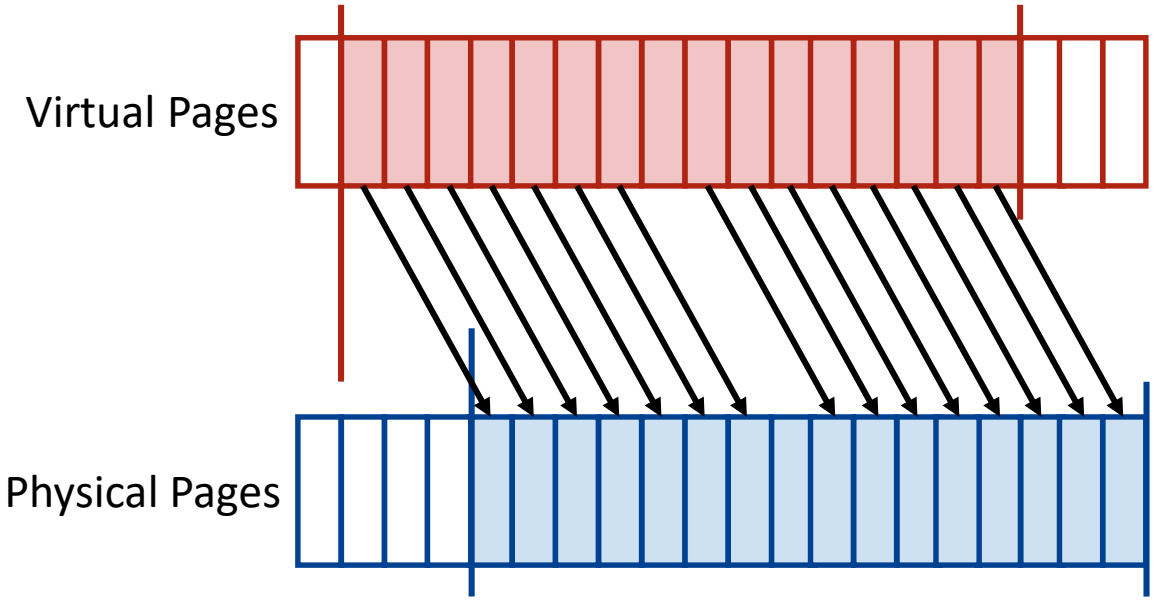

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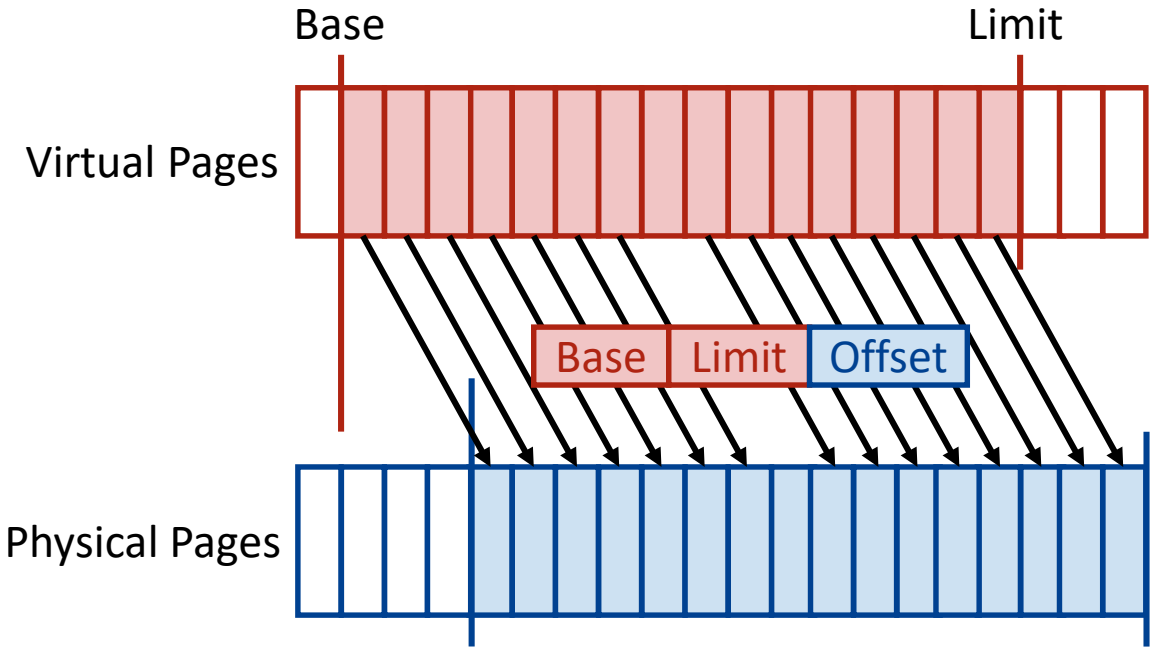

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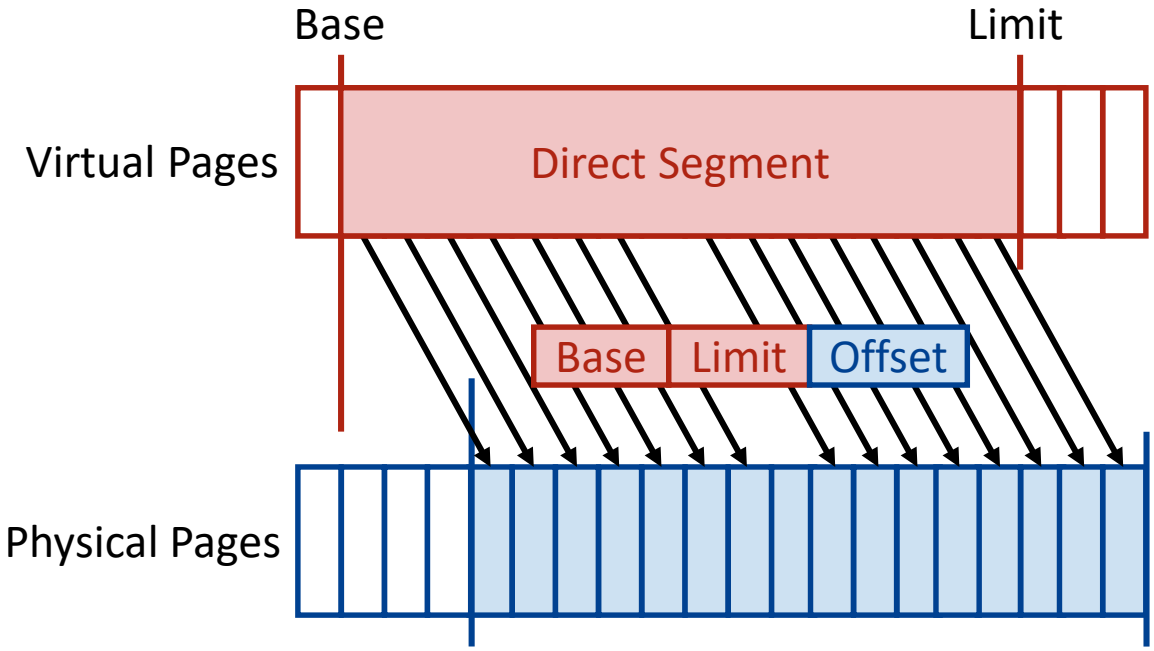

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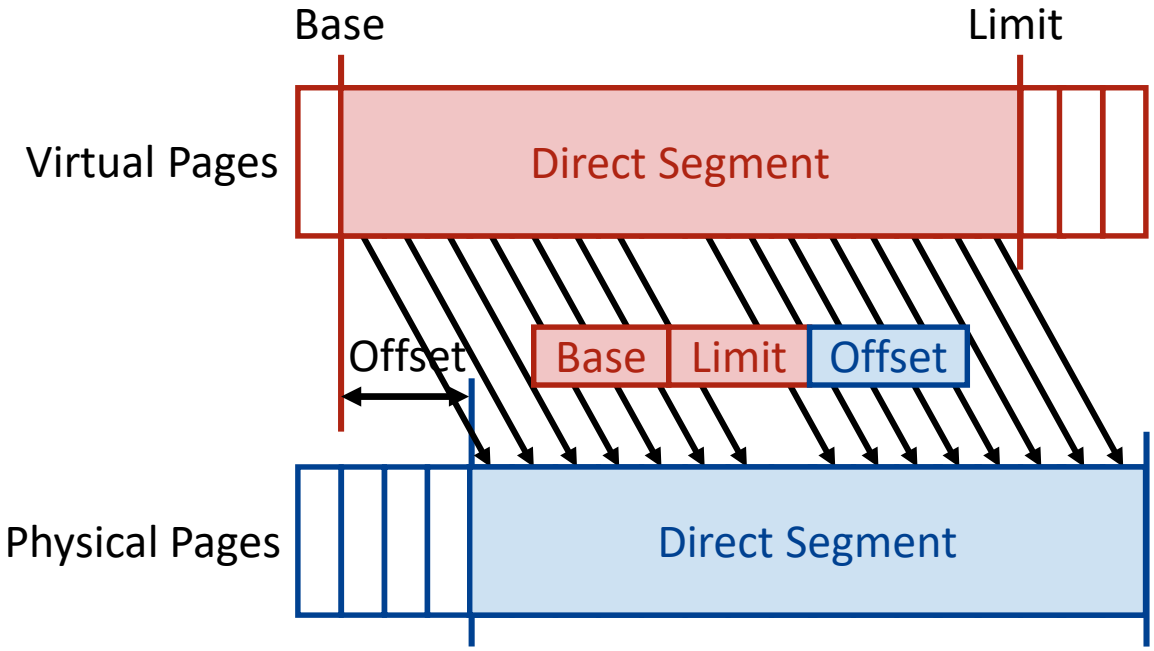

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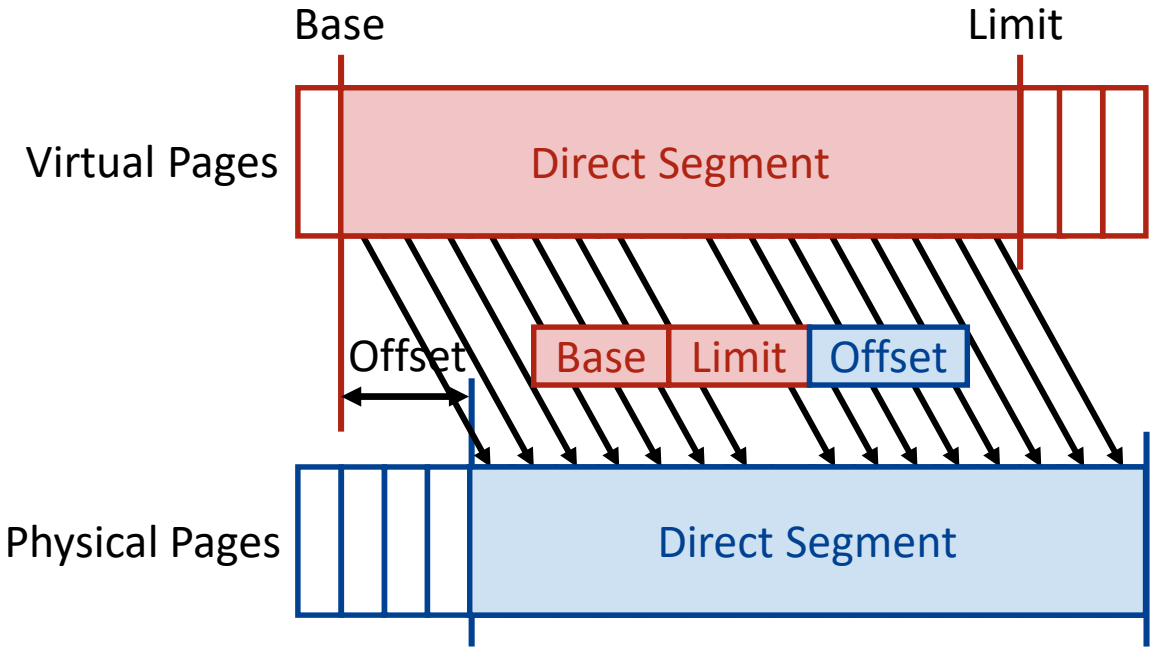

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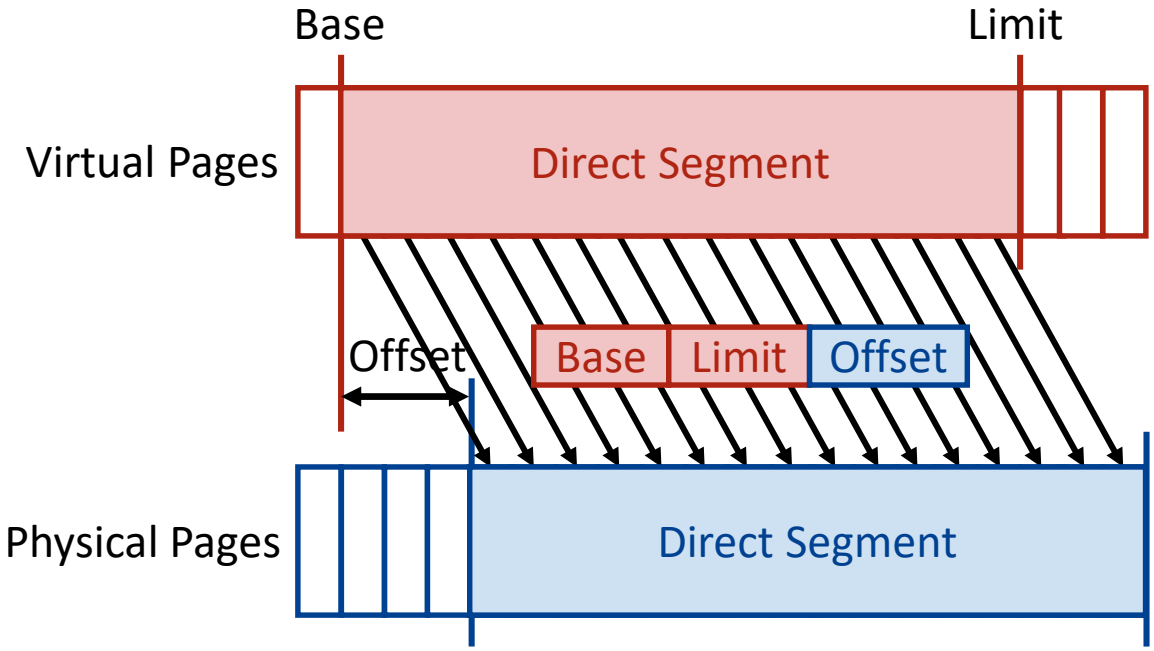

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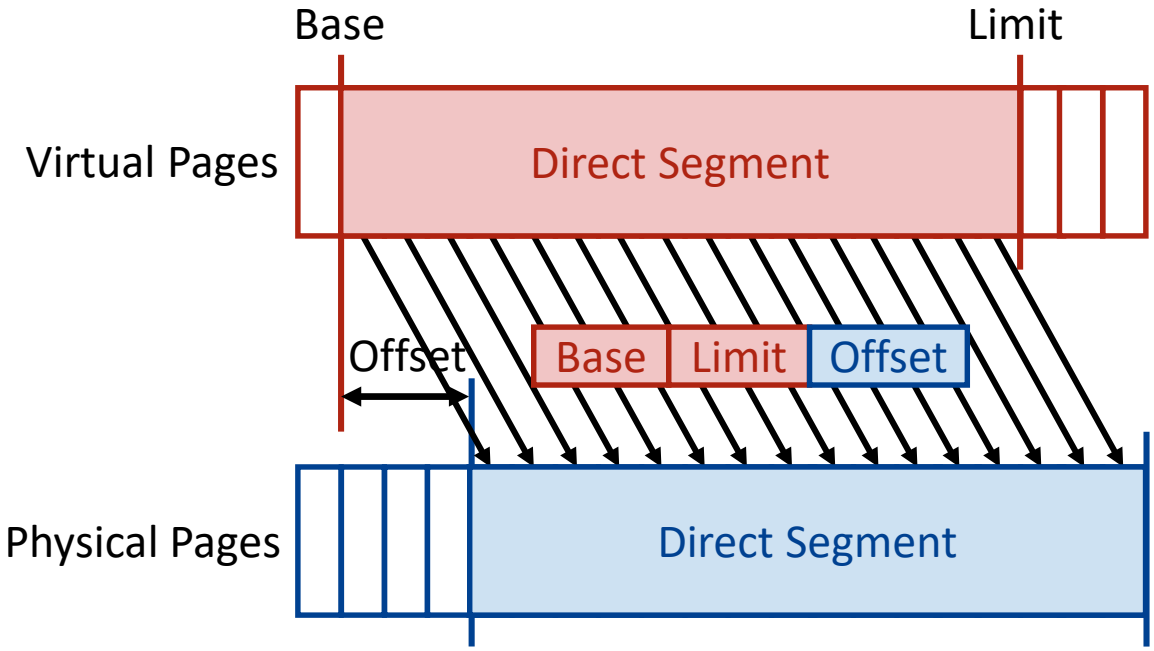

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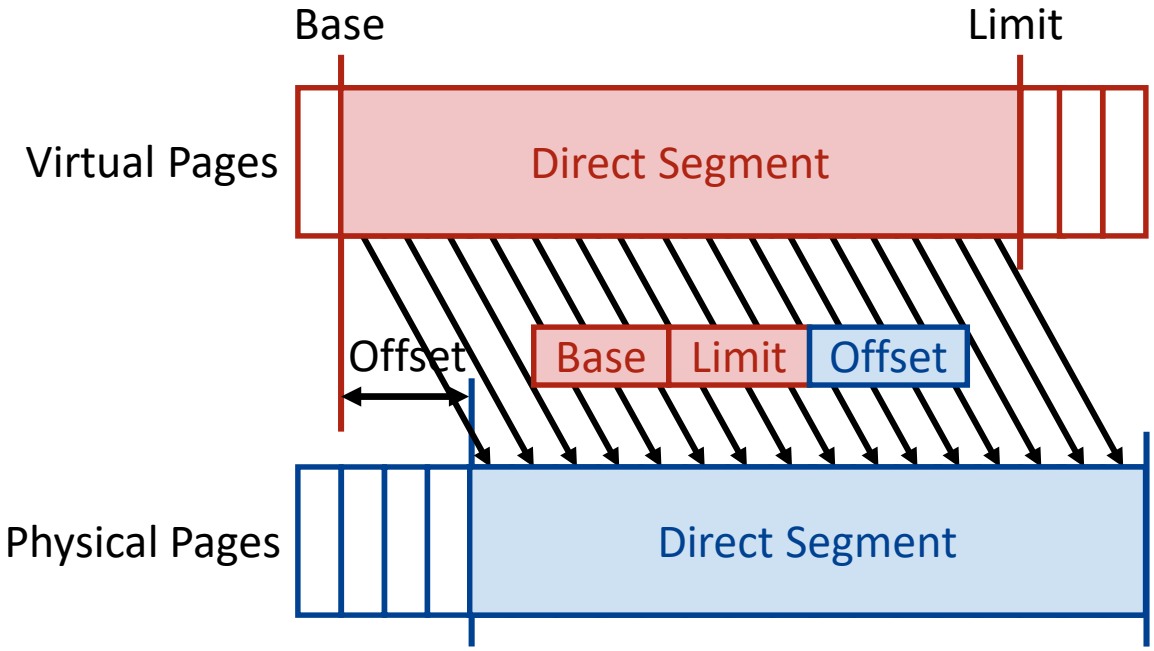

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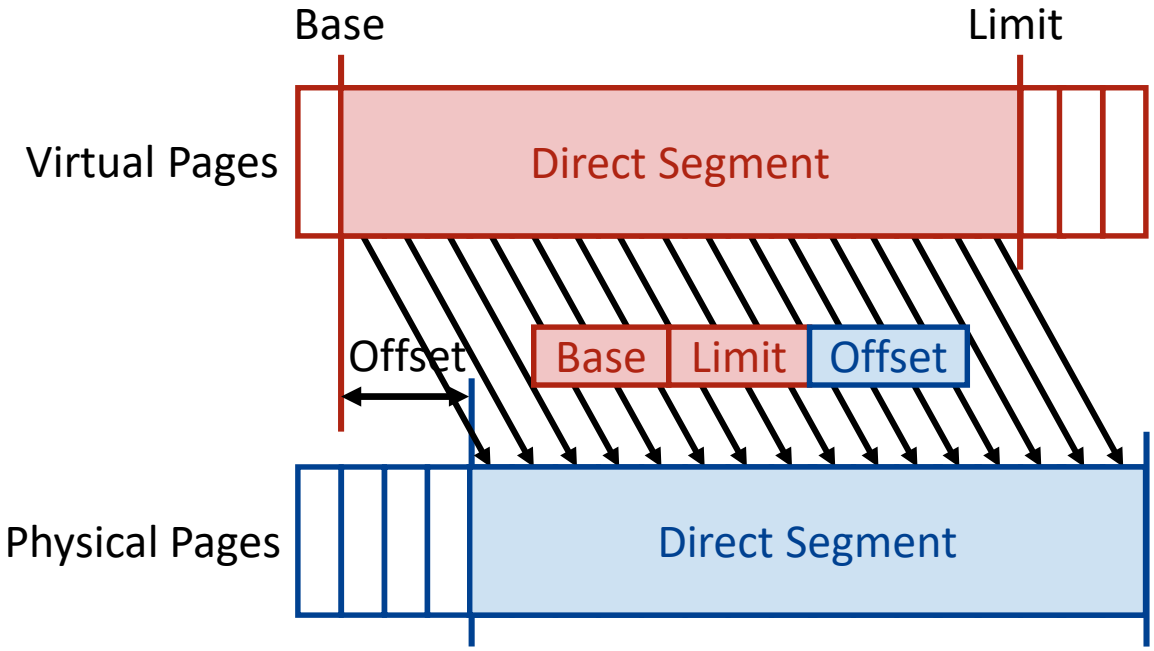

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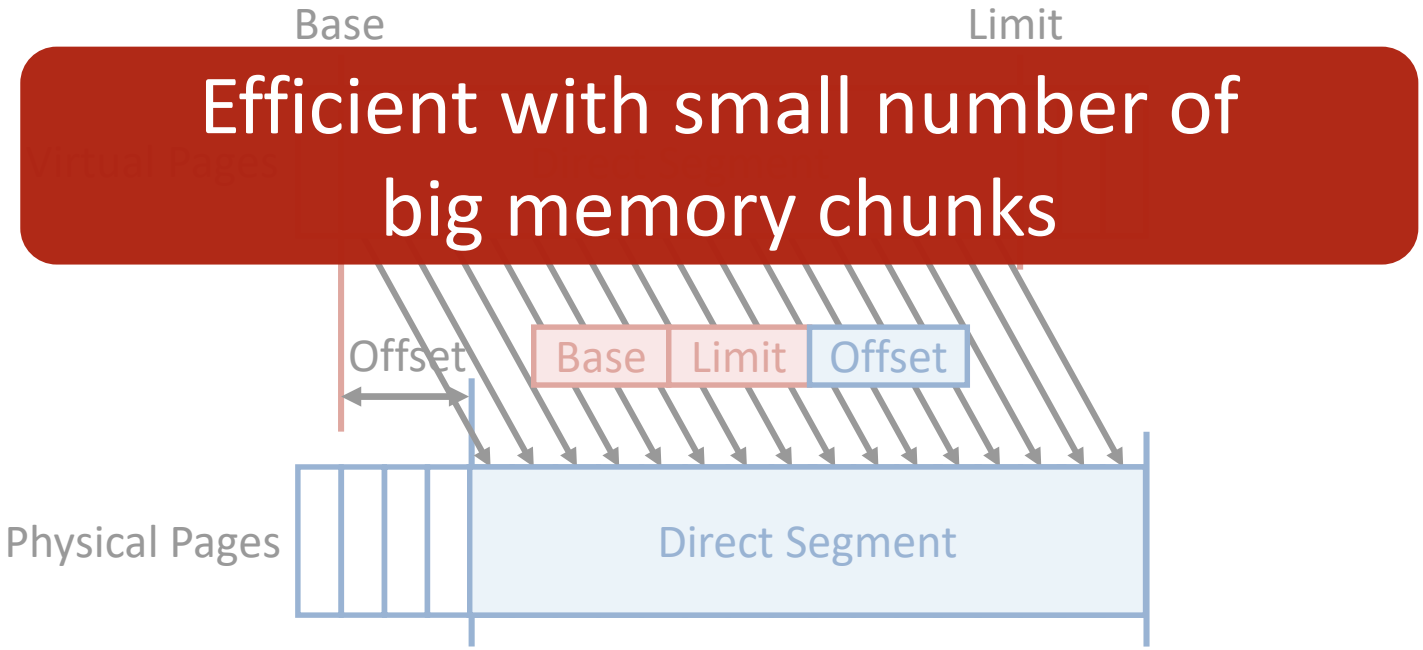

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- Cluster TLB
  - Affinity for clustering of mapping of up to 8 pages
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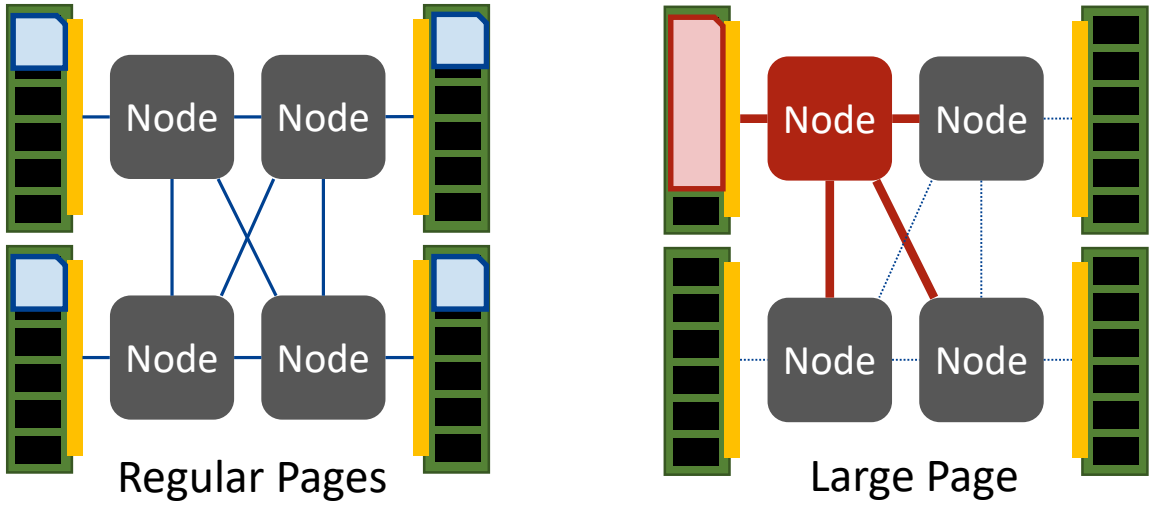
Prior proposals efficiently support **specific** memory mapping scenarios

Large Contiguity vs. Memory Non-Uniformity



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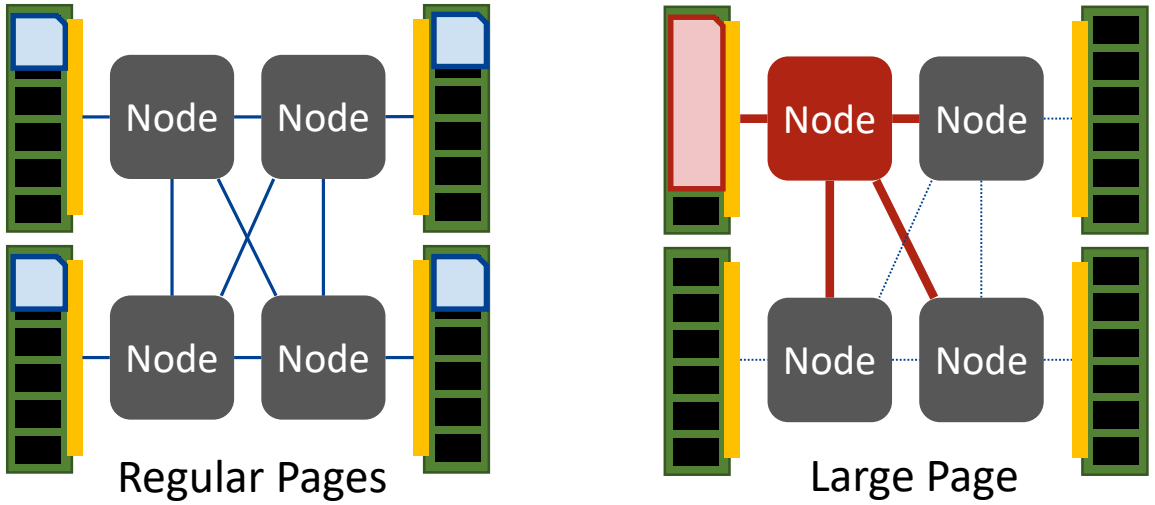

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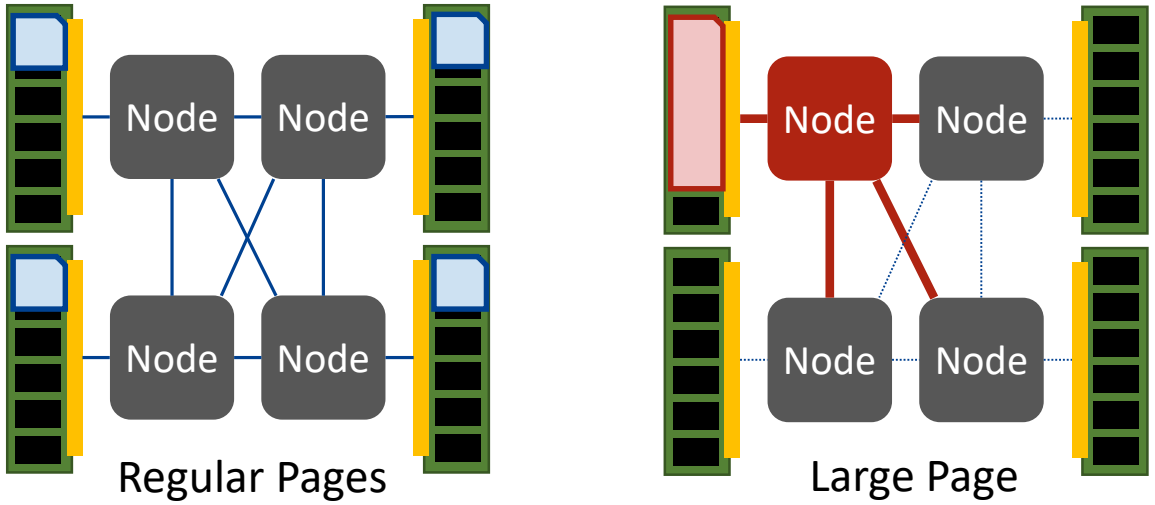

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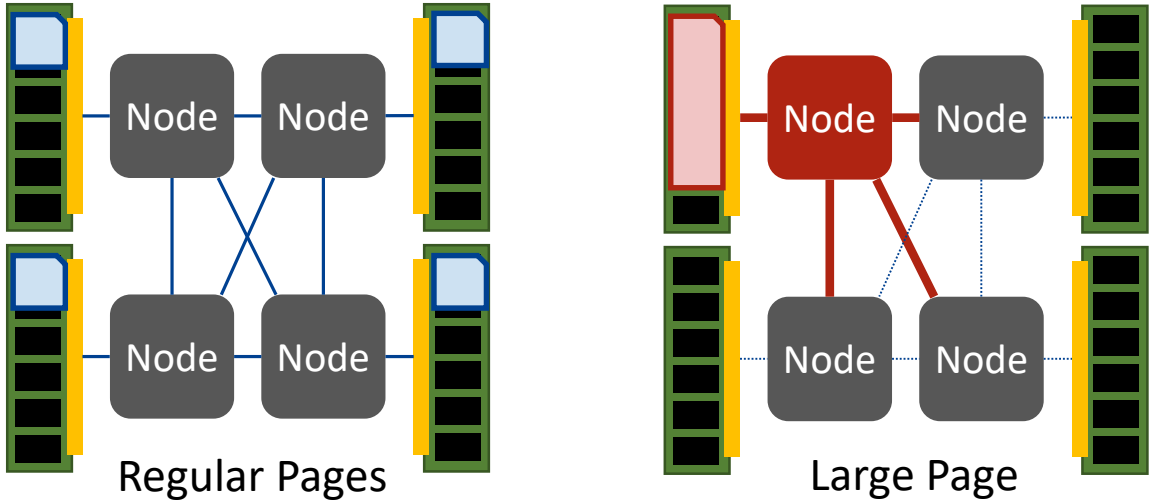

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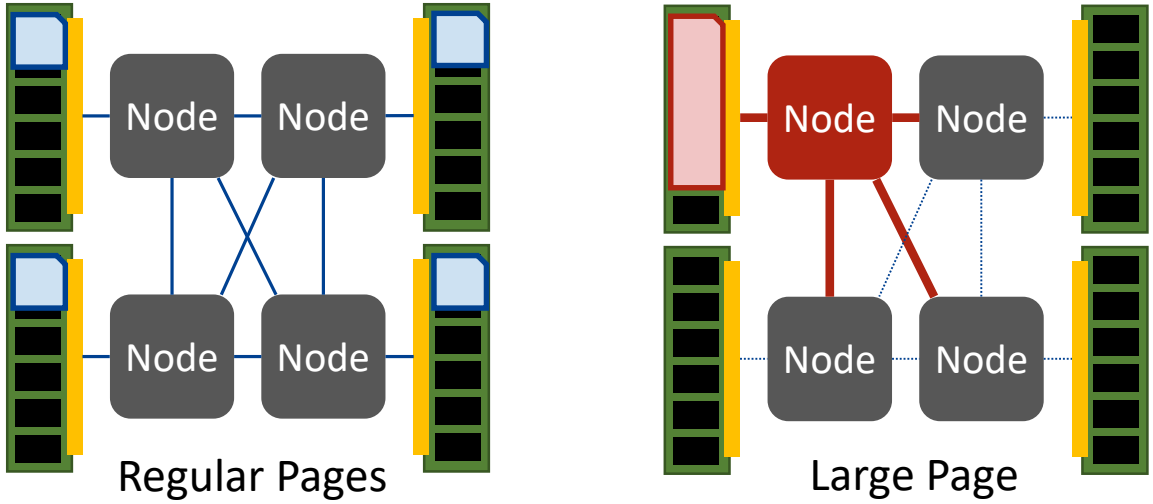

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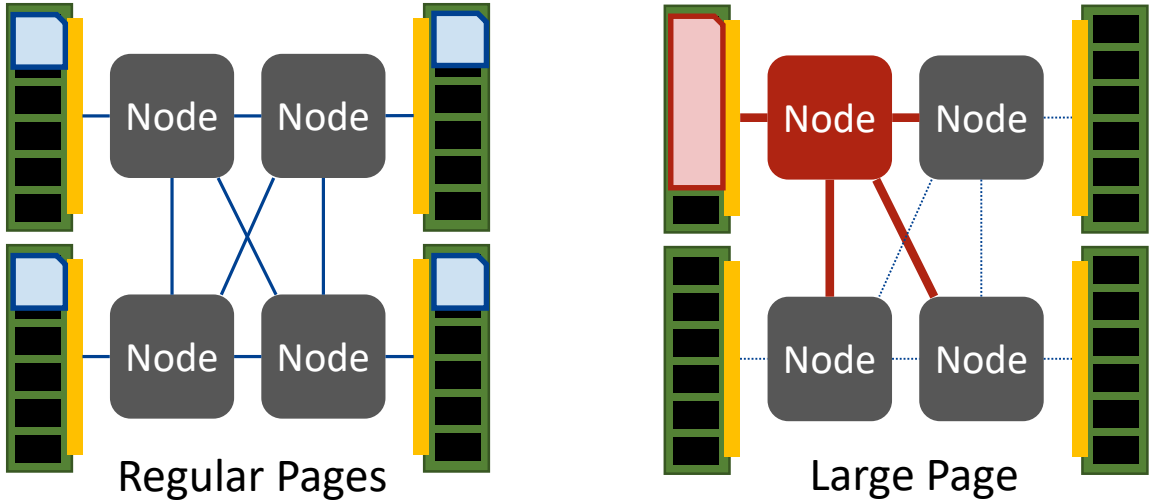

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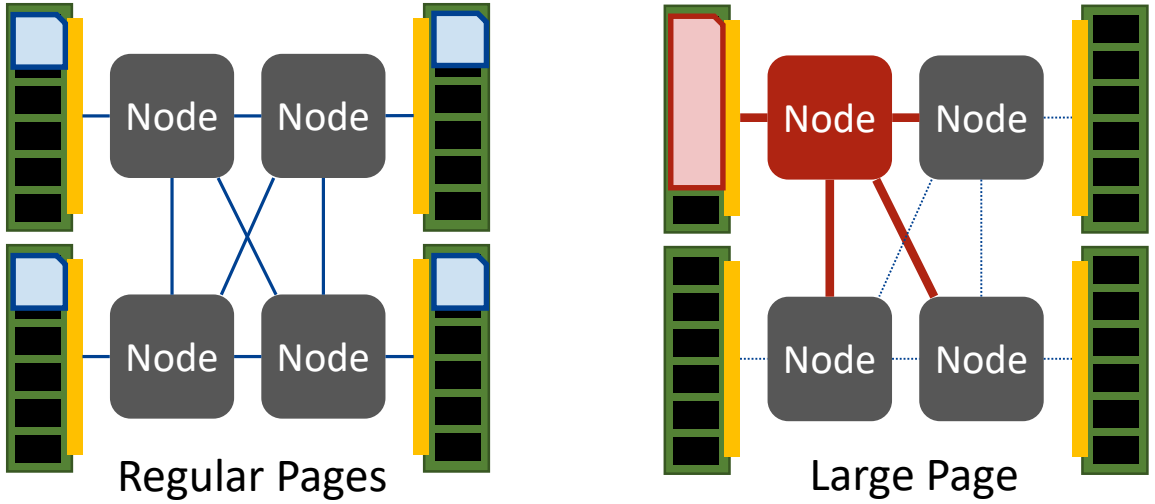

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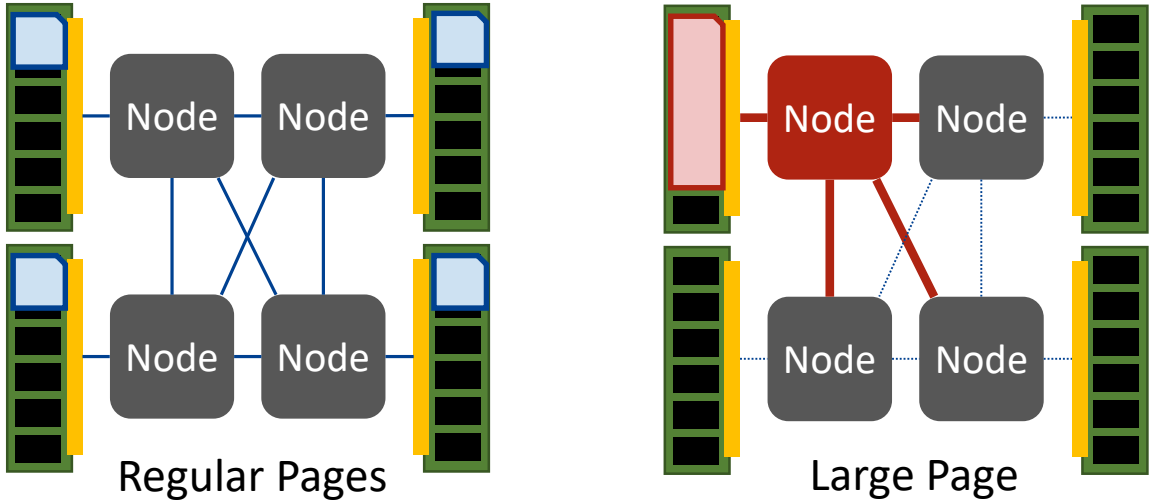

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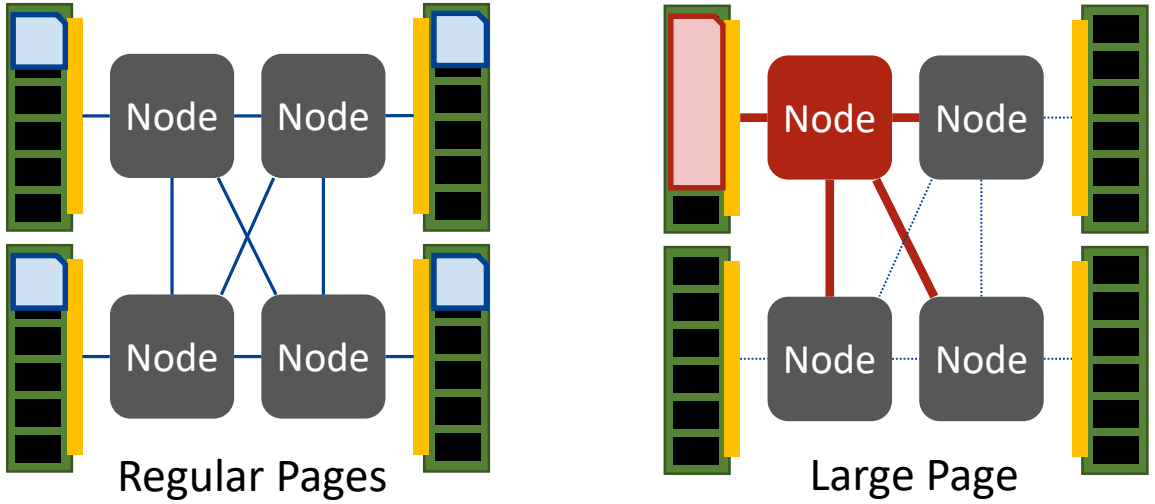

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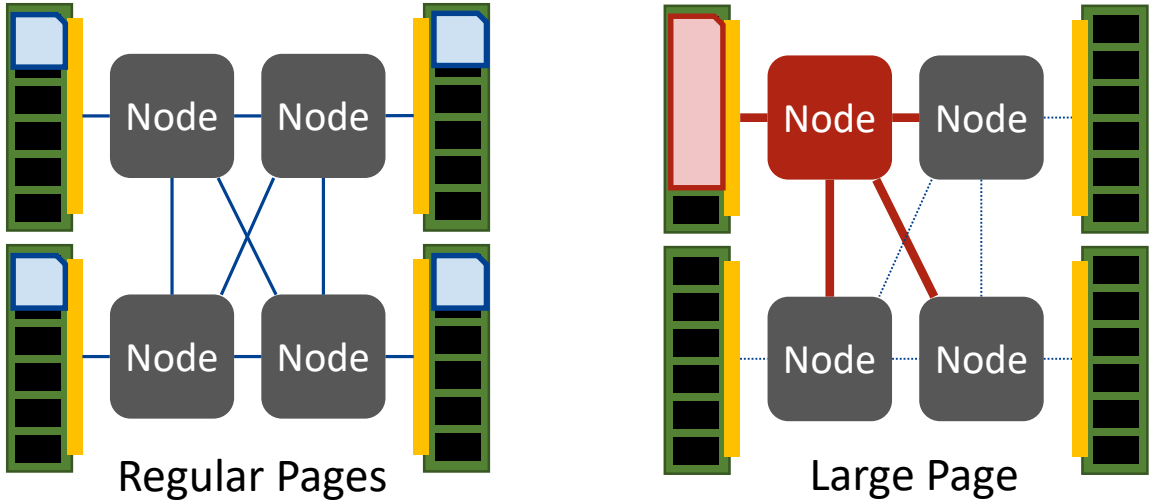

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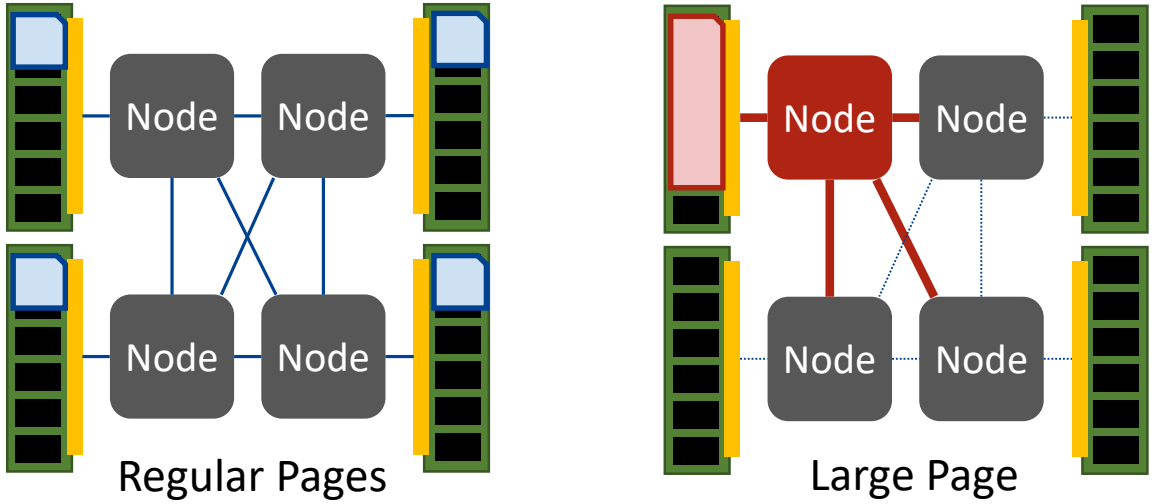

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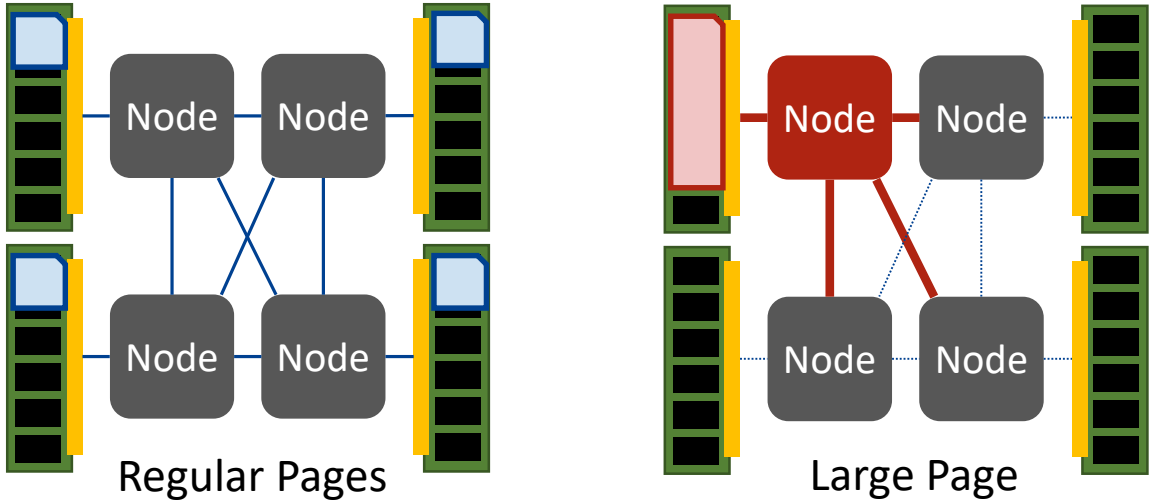

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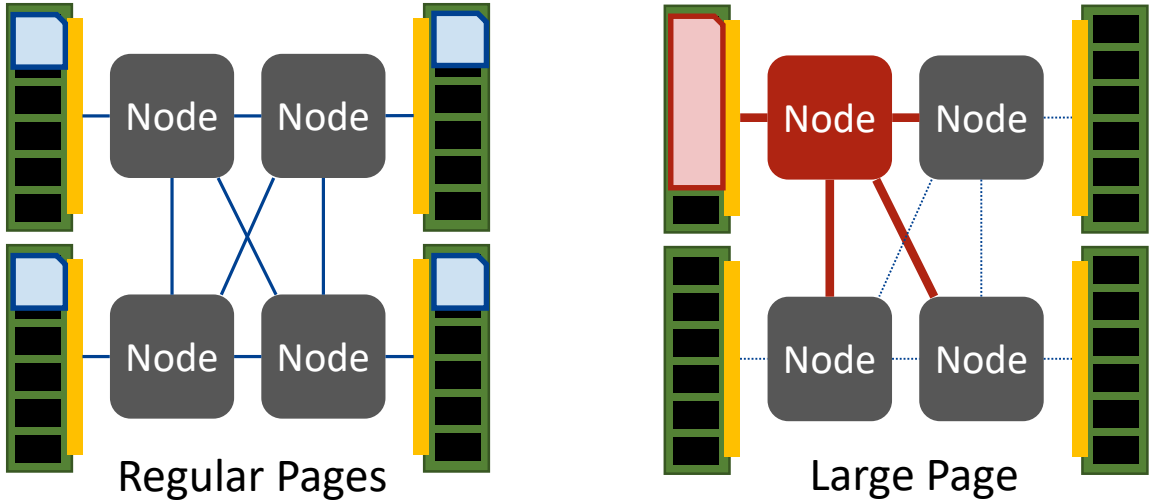

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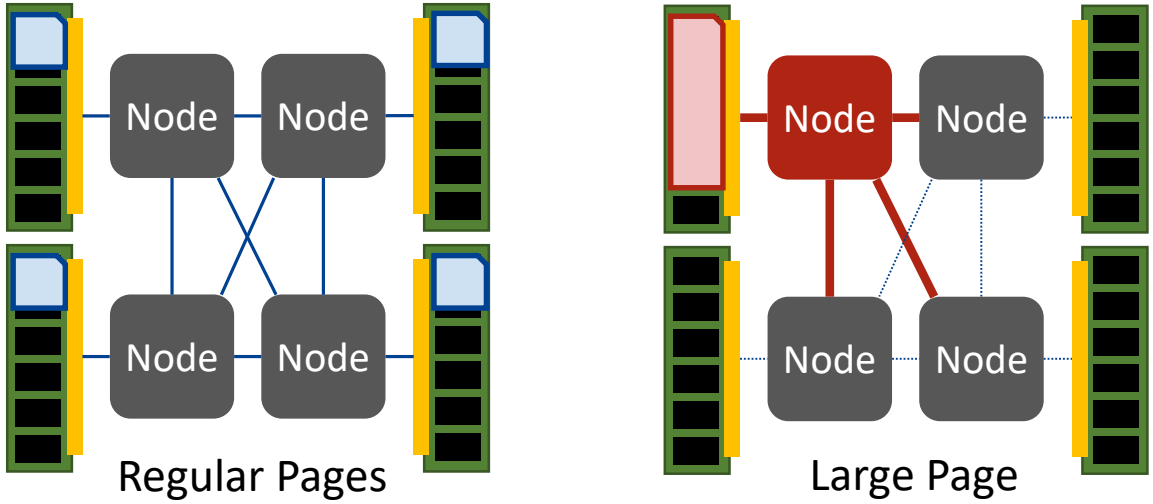

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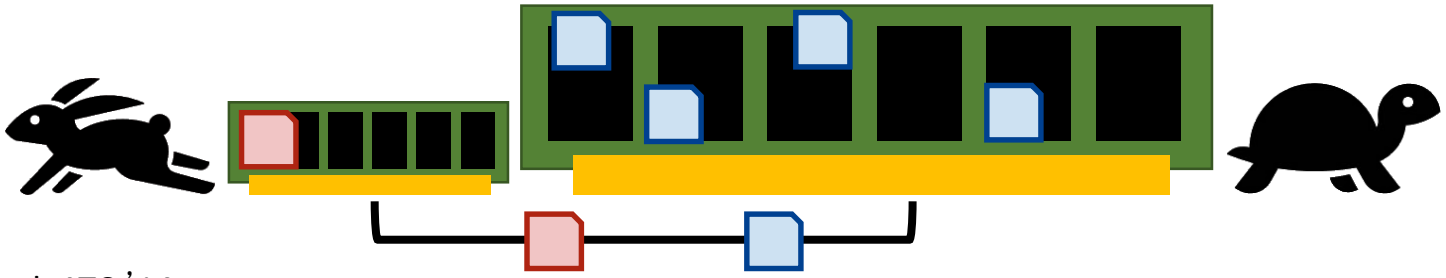

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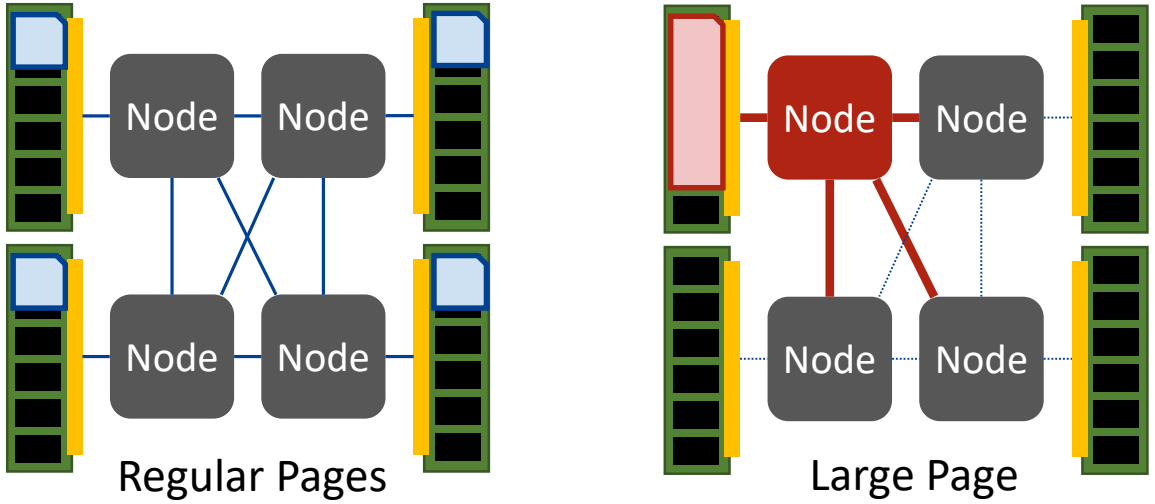

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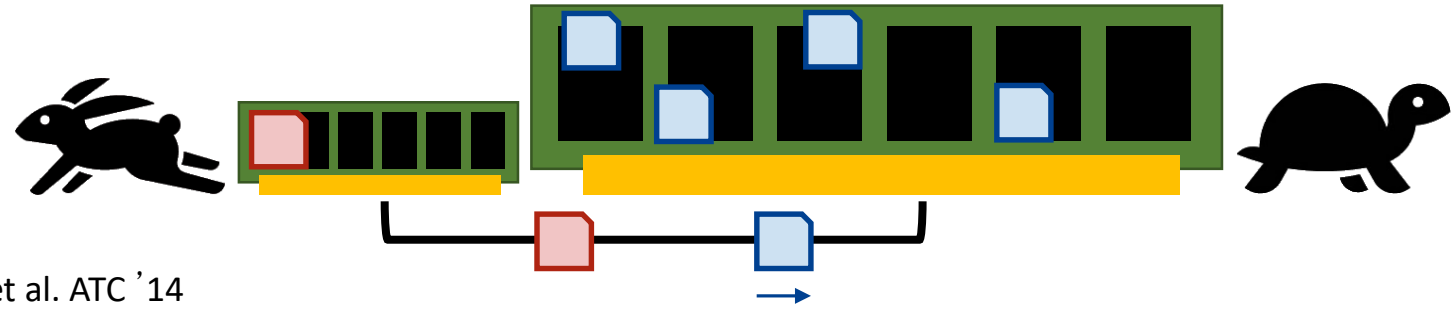

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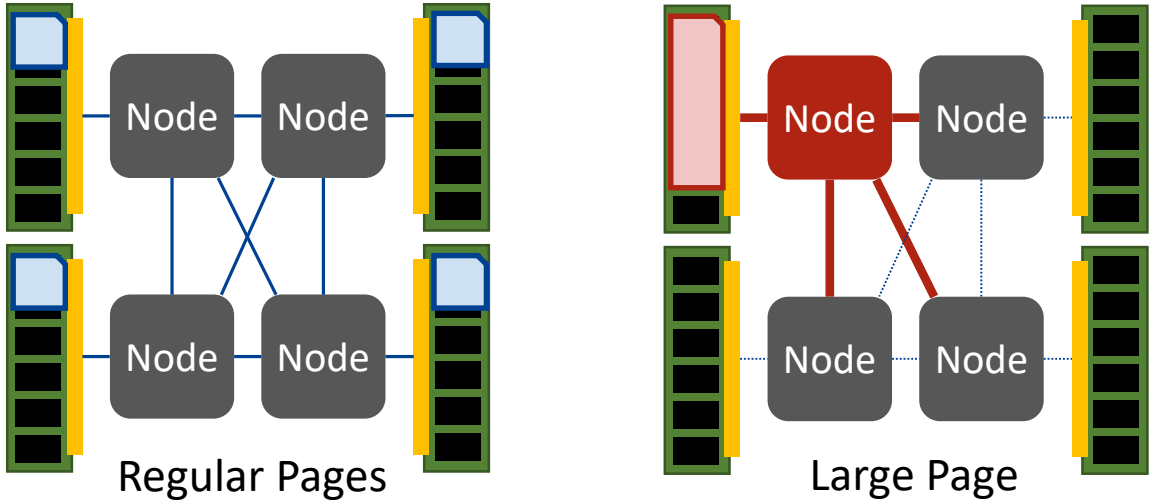

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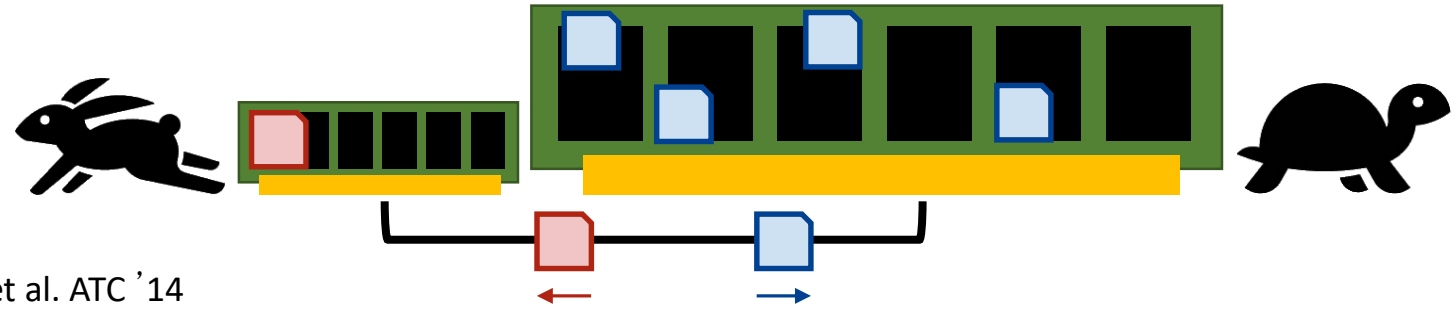

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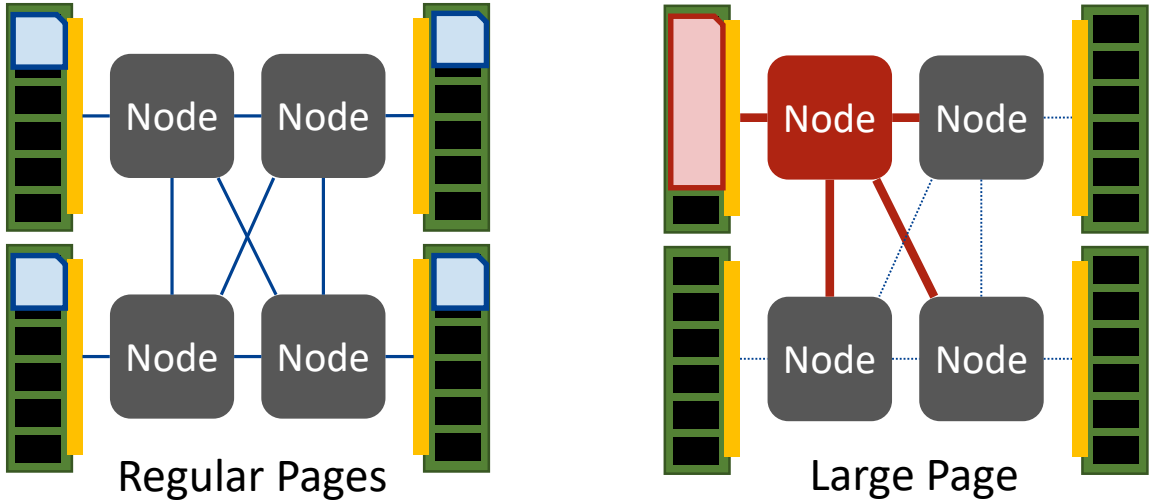

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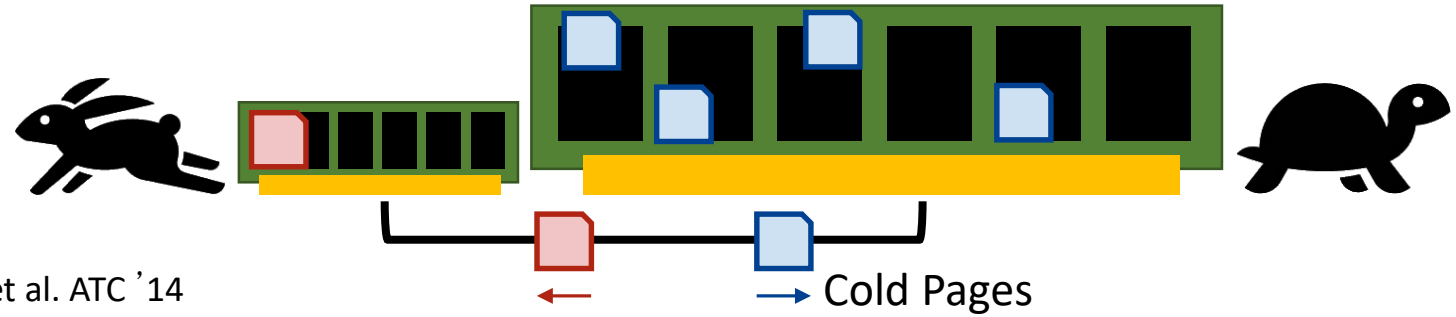

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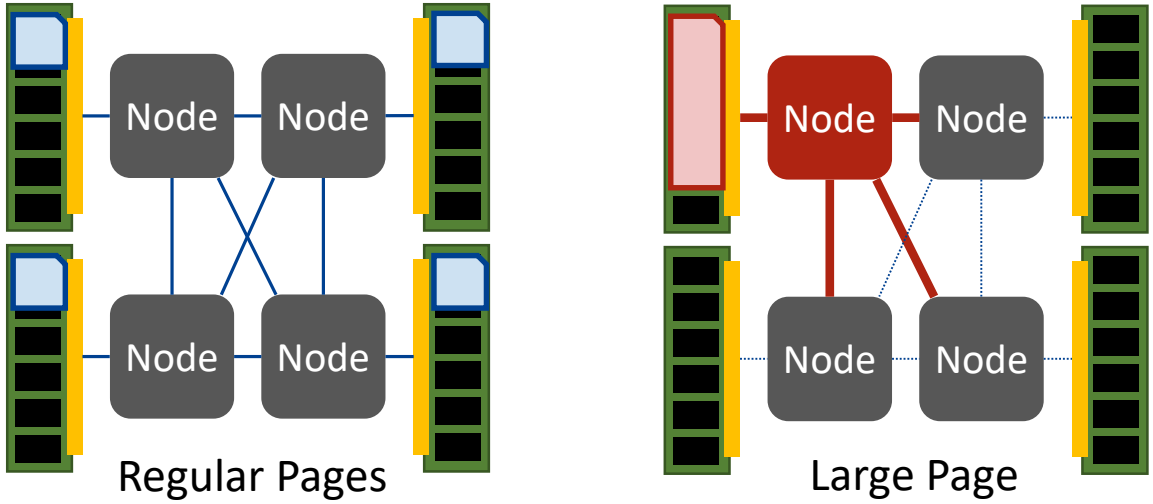

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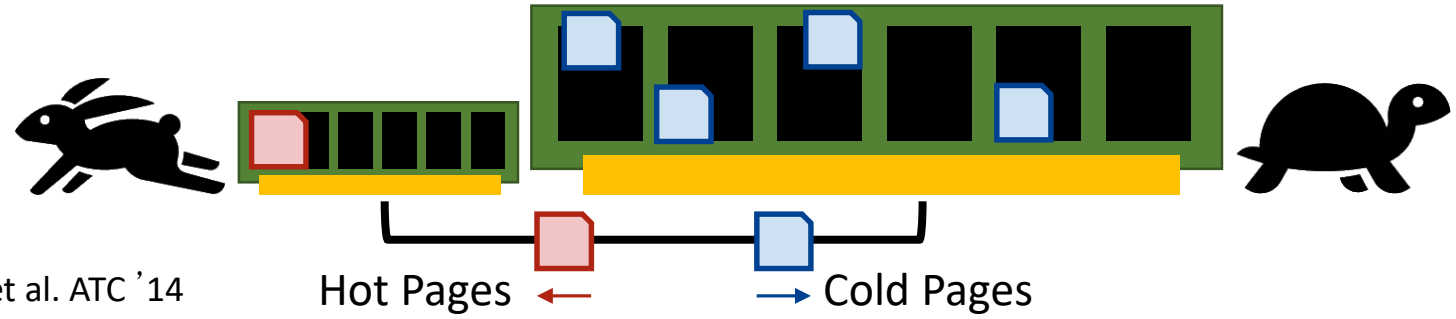

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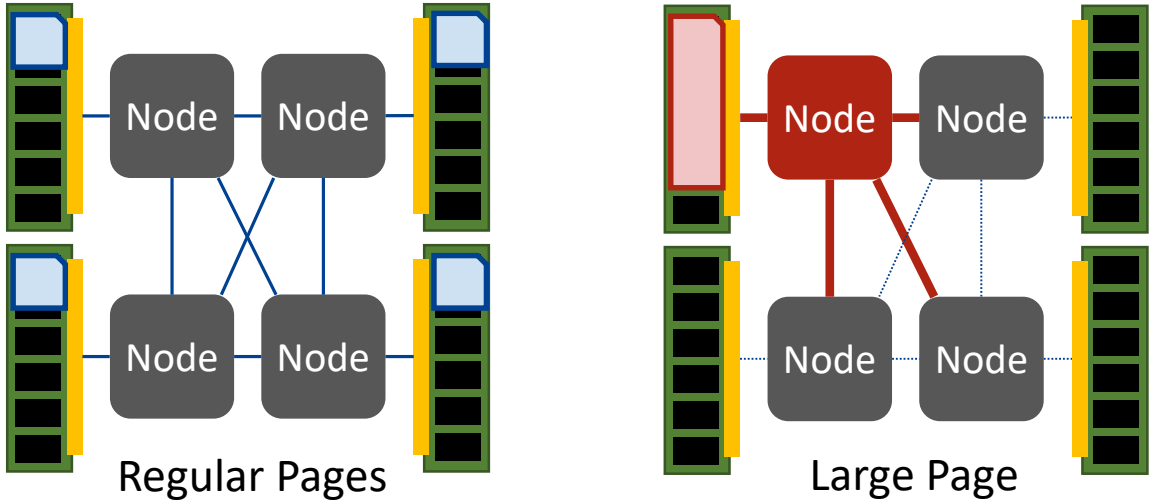

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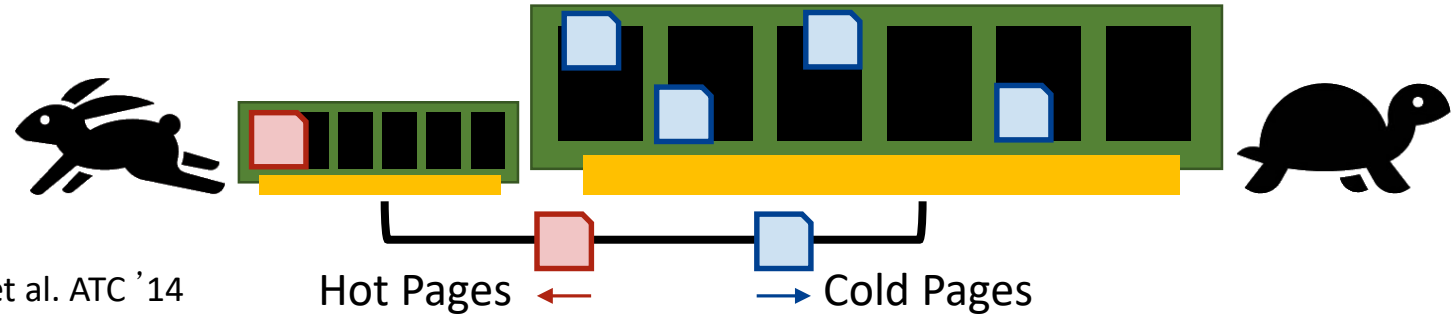

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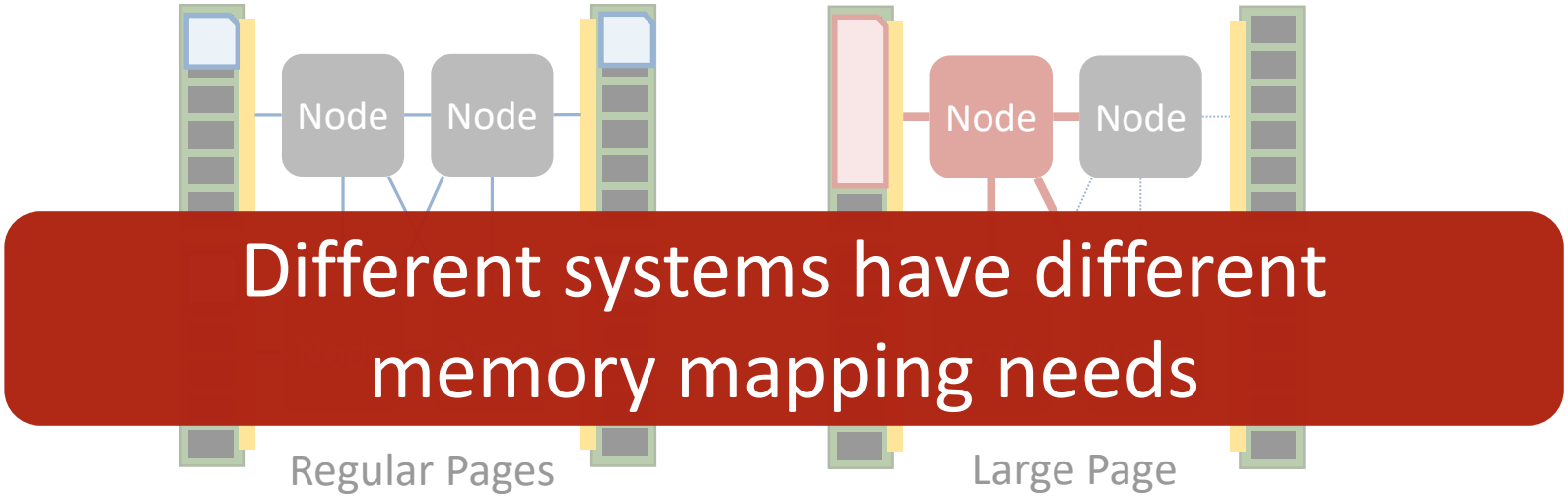

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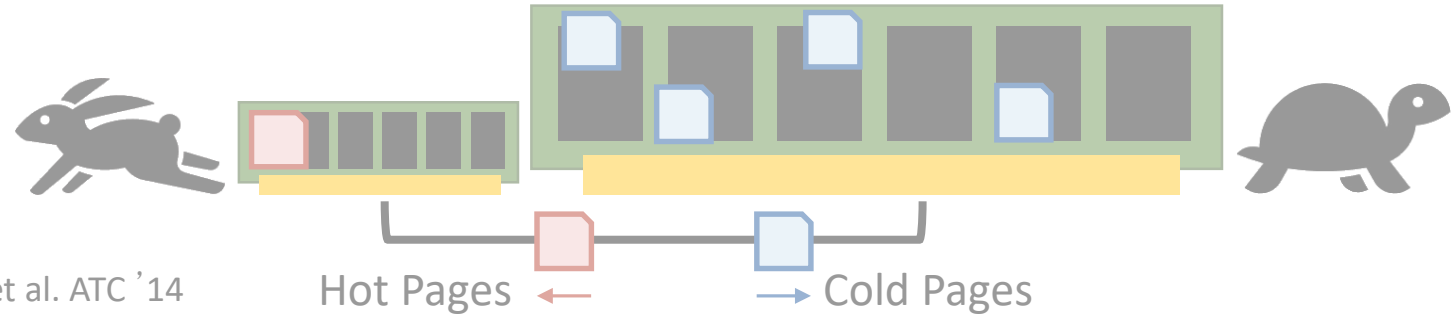

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- Contiguity distribution varies among workloads
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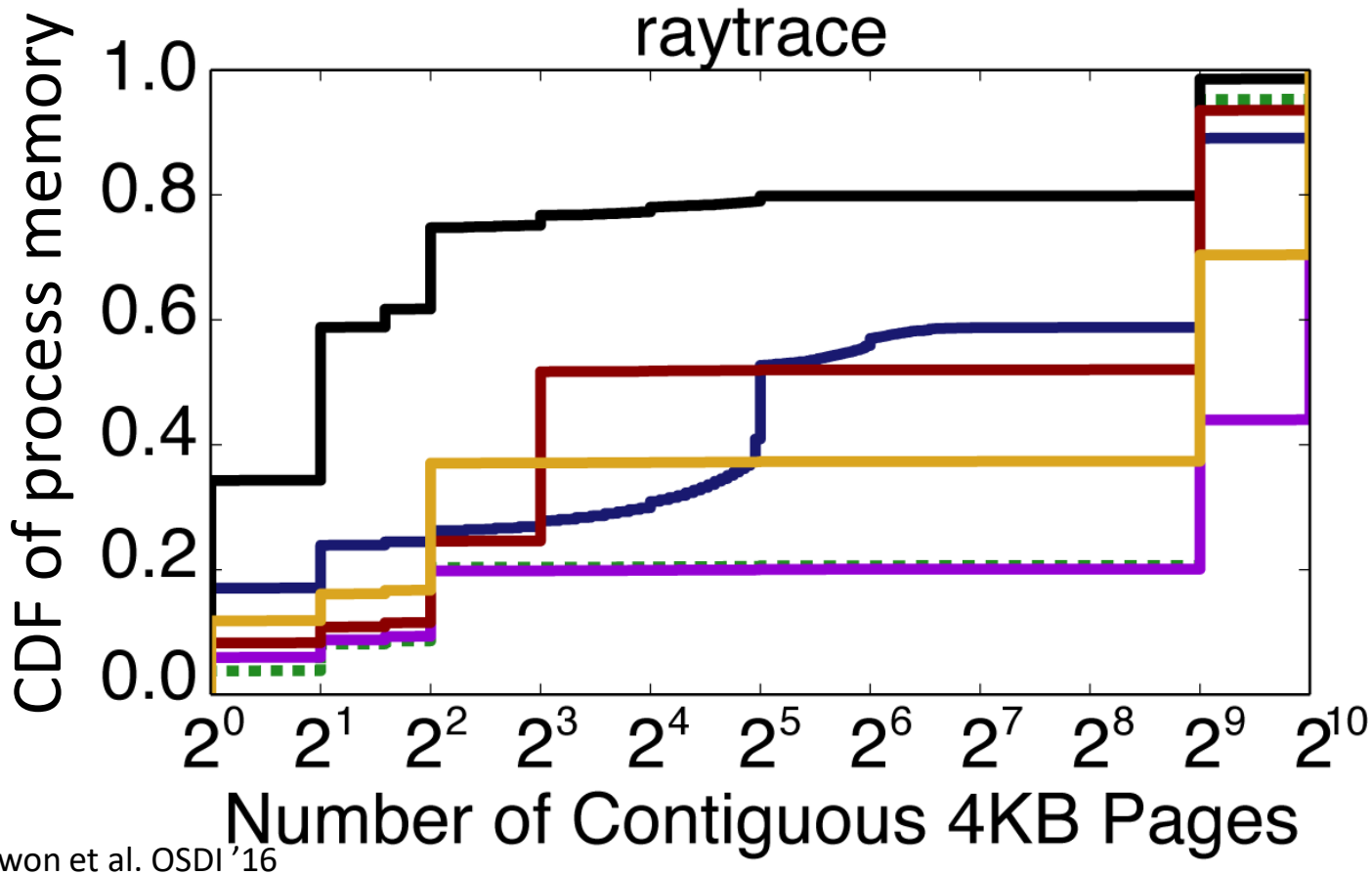

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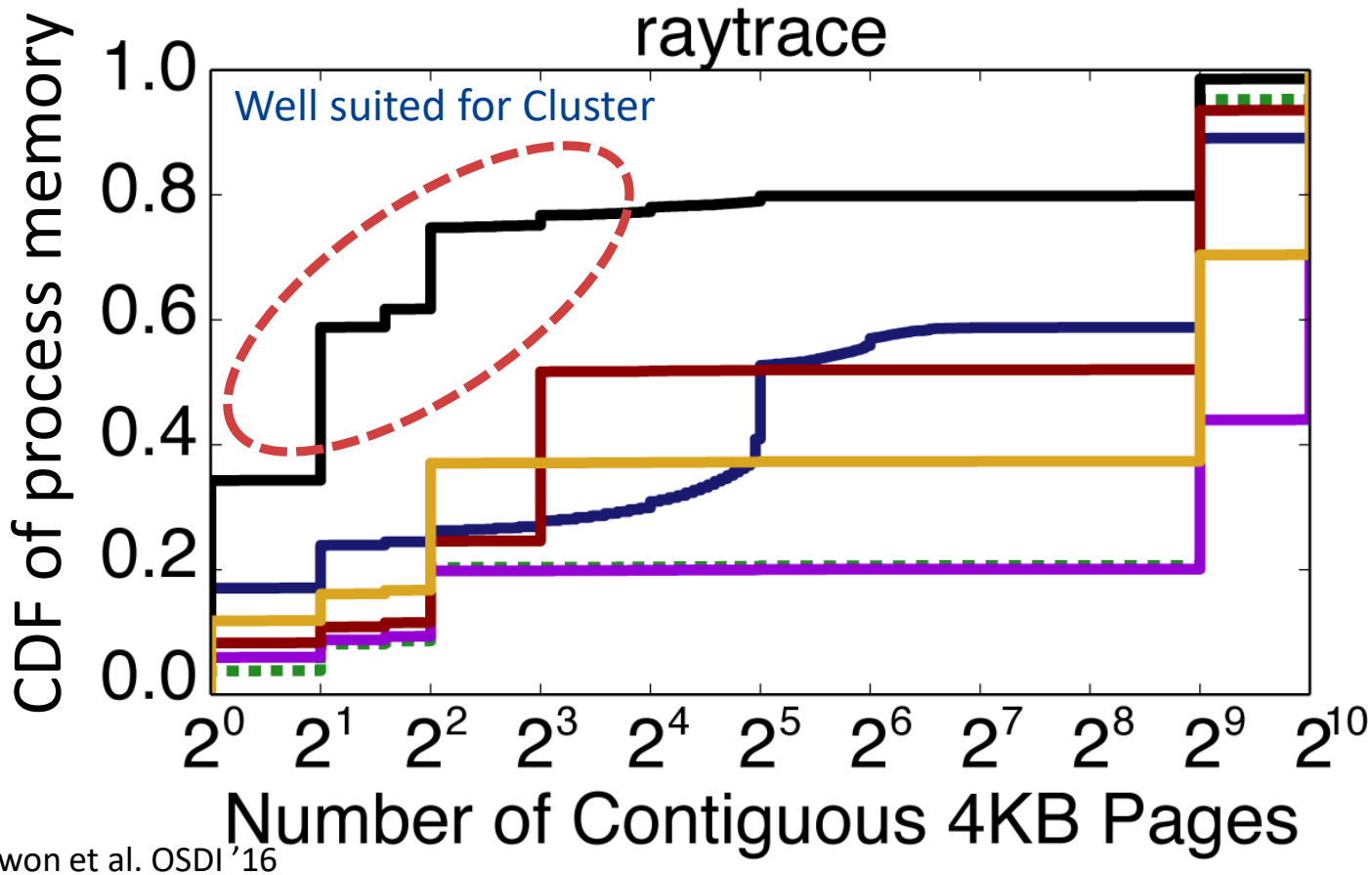

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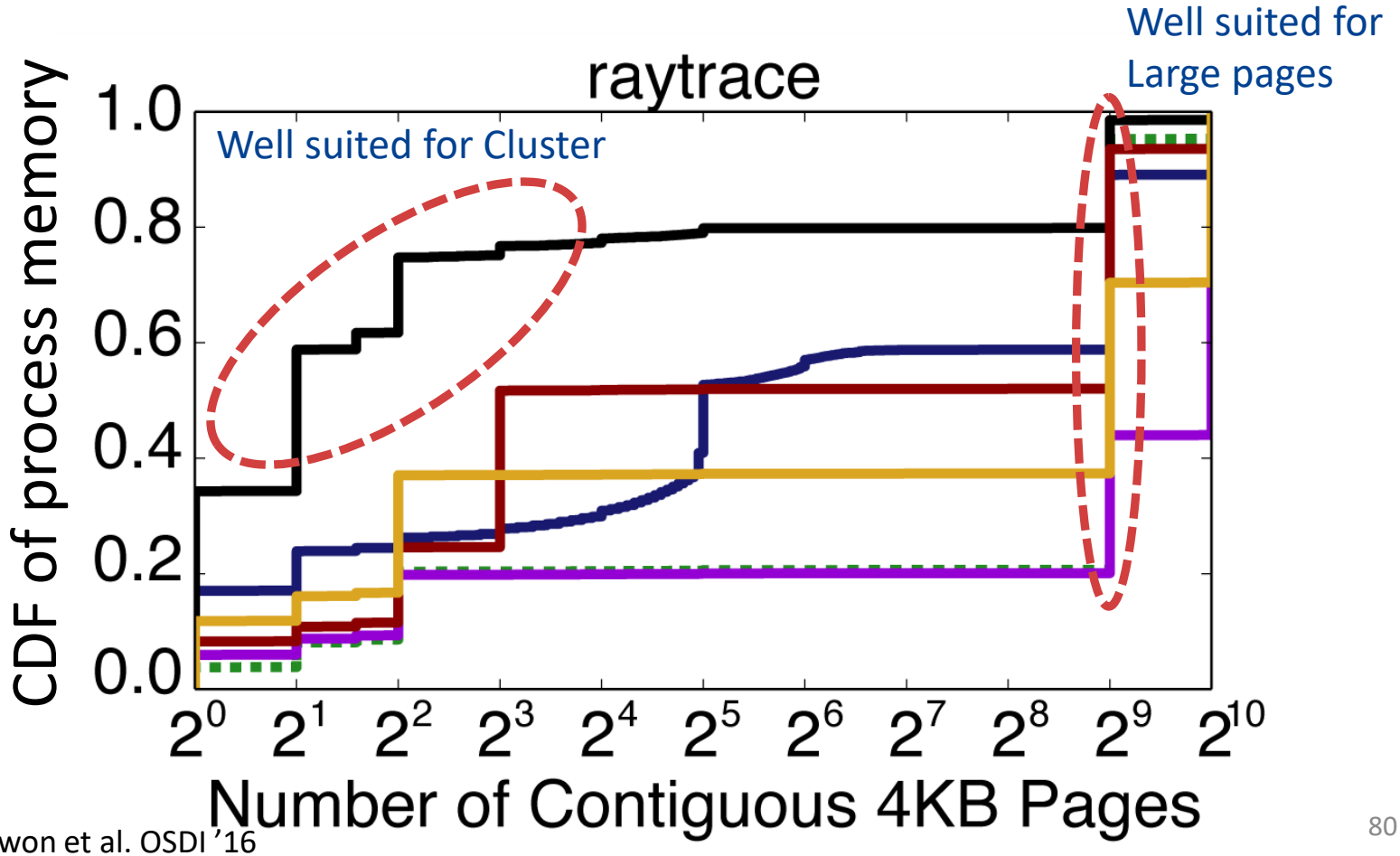

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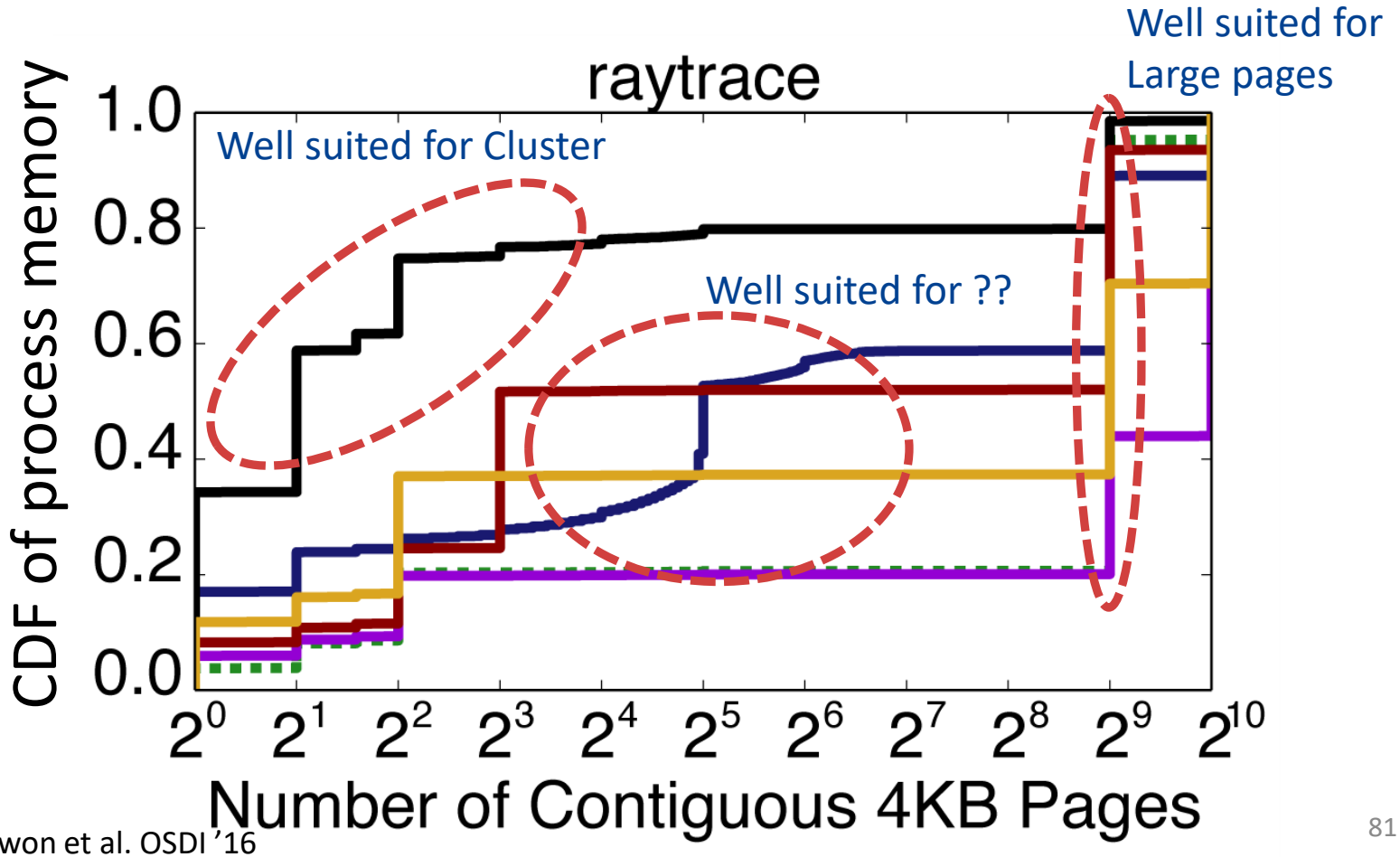

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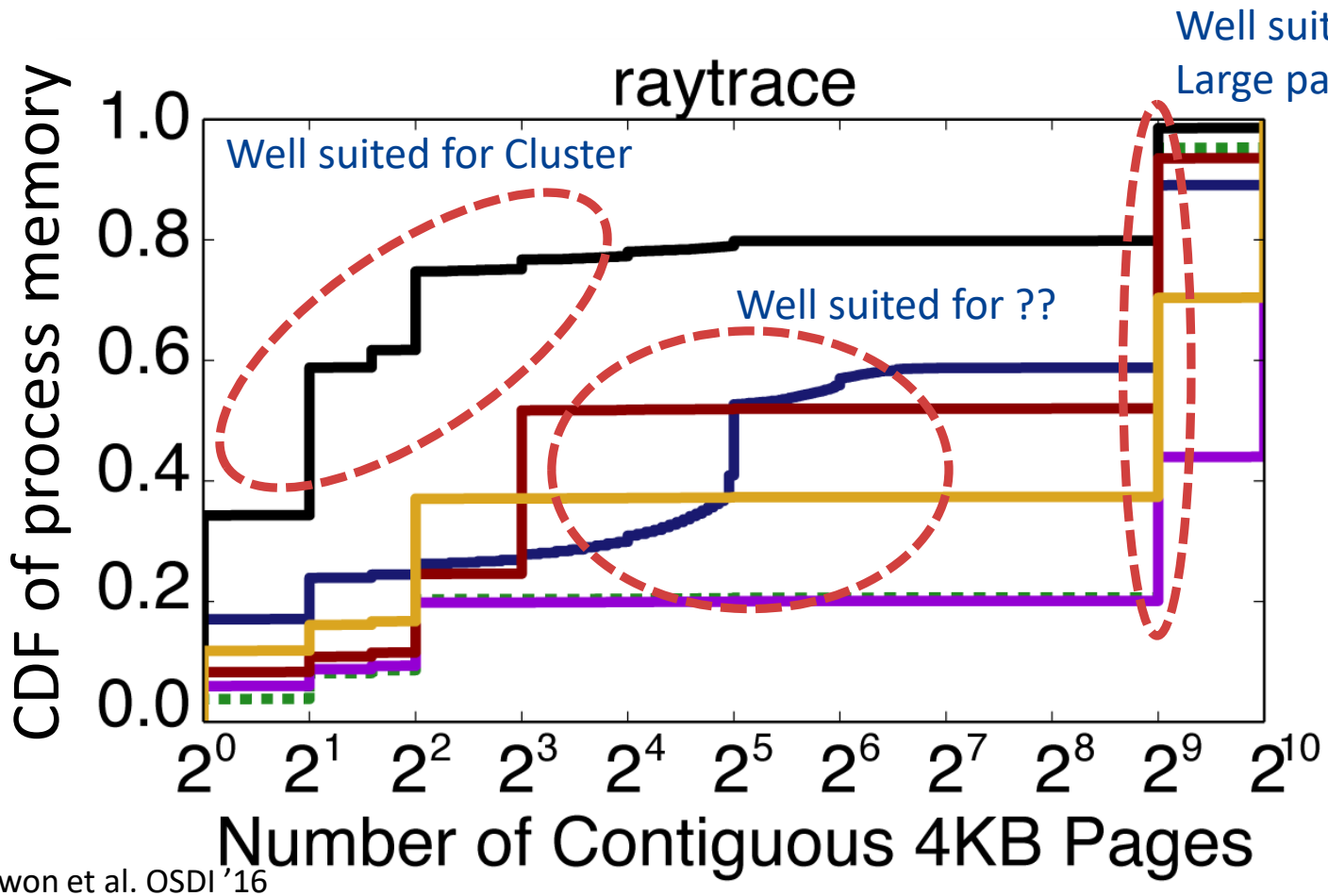

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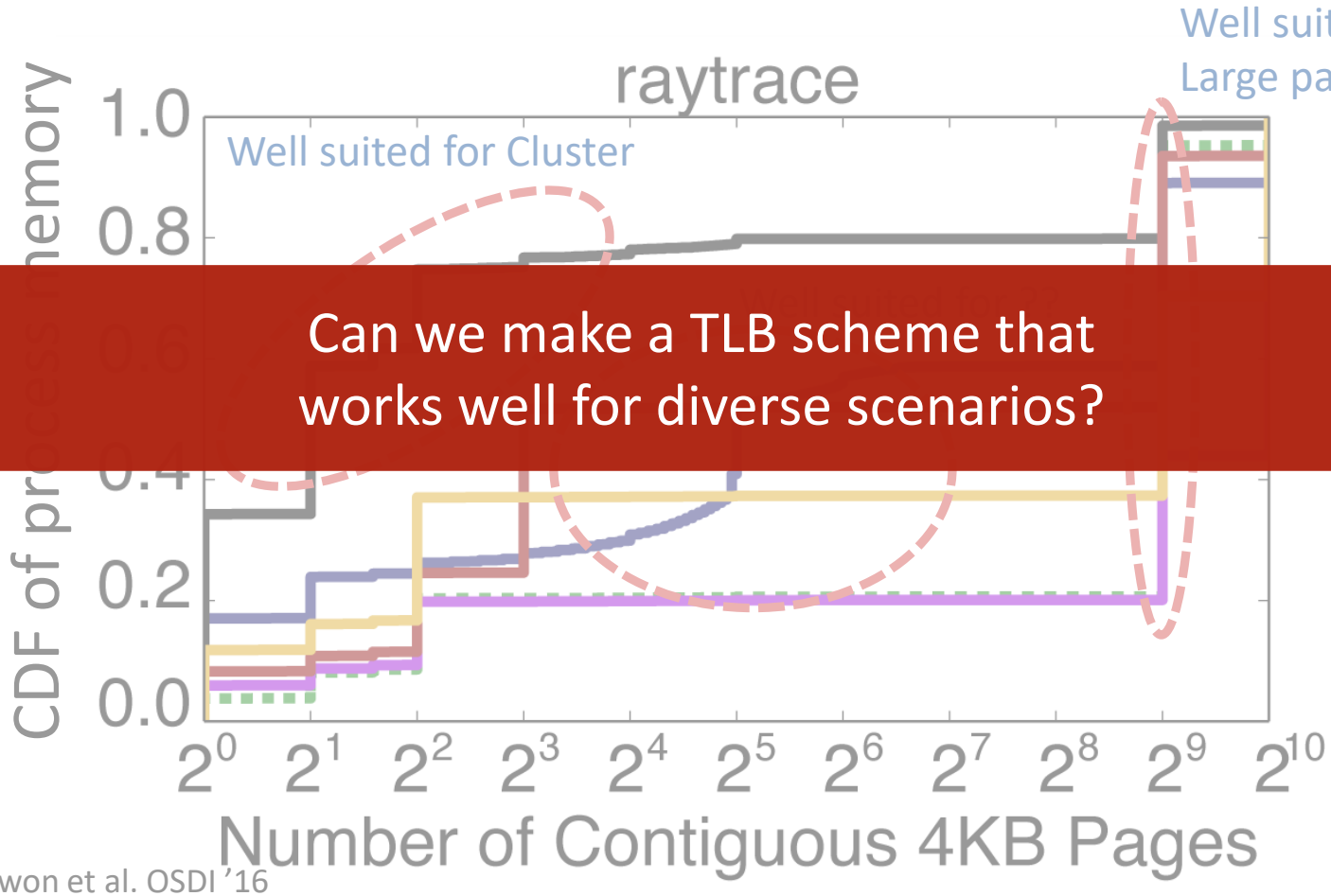

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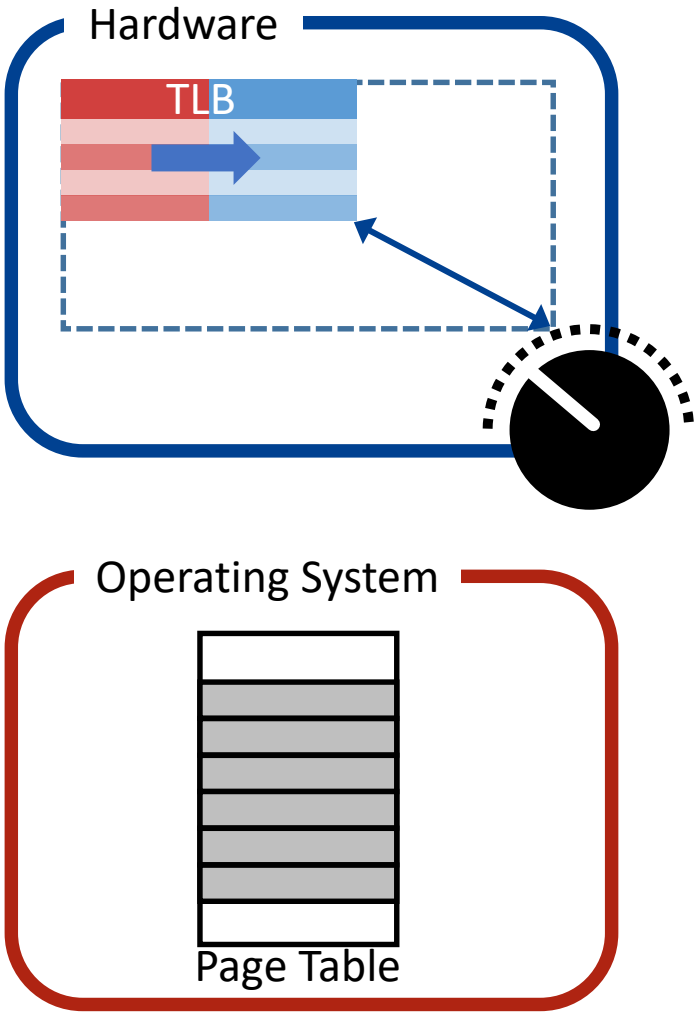

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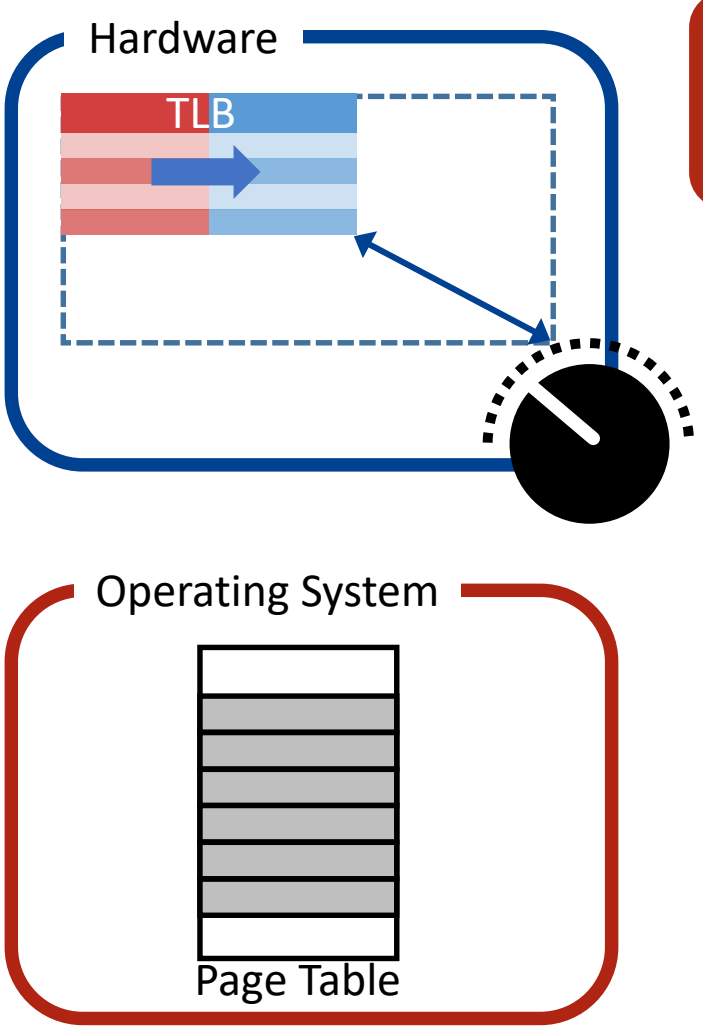

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- **HW**-**SW** Joint Effort
- **HW** offers adjustable TLB coverage
  - Number of TLB entries fixed
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- **OS** decides best TLB coverage
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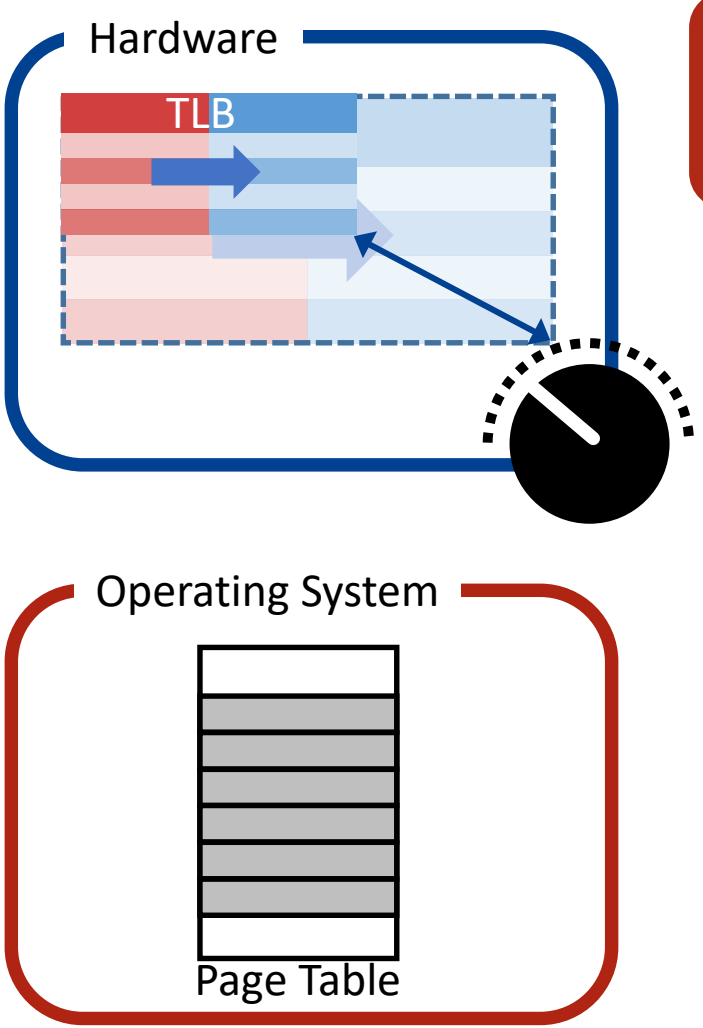

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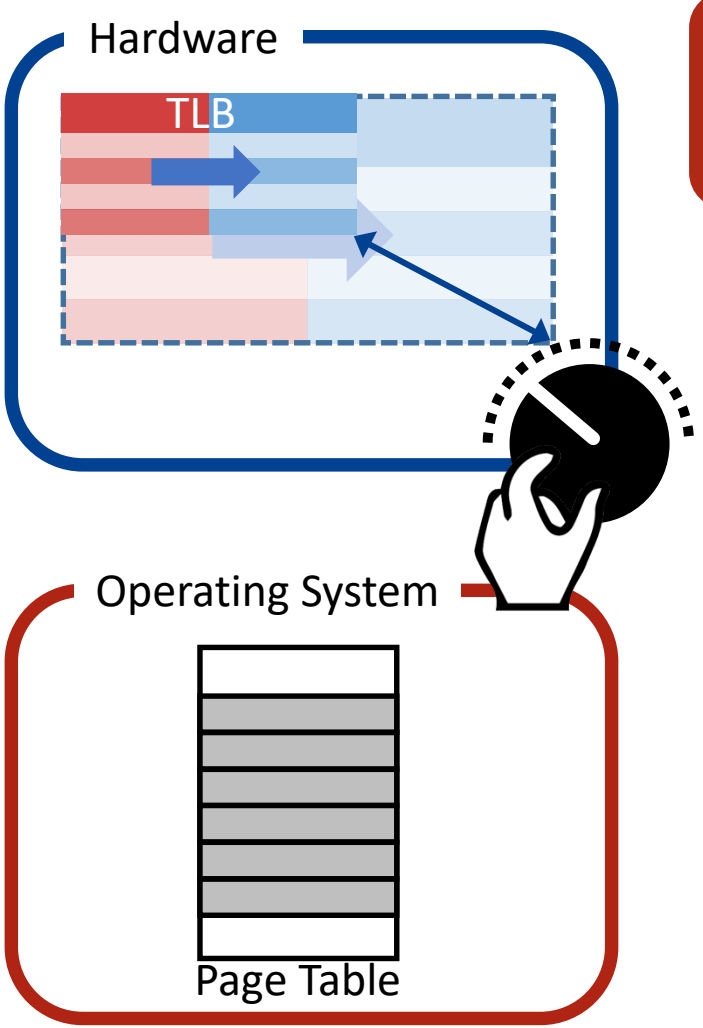

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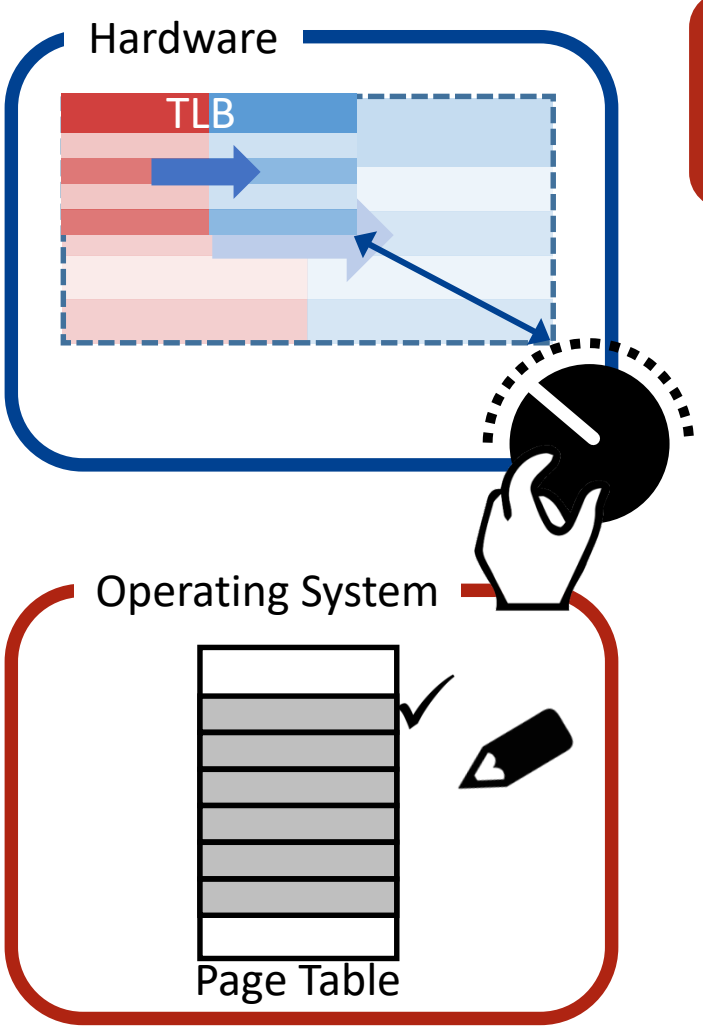

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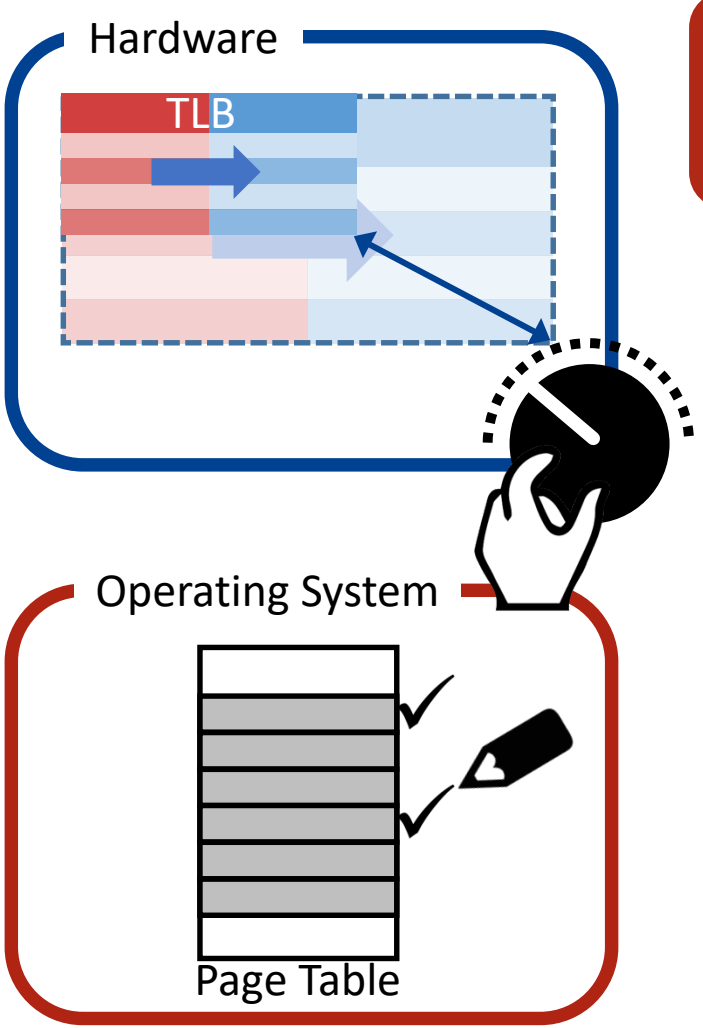

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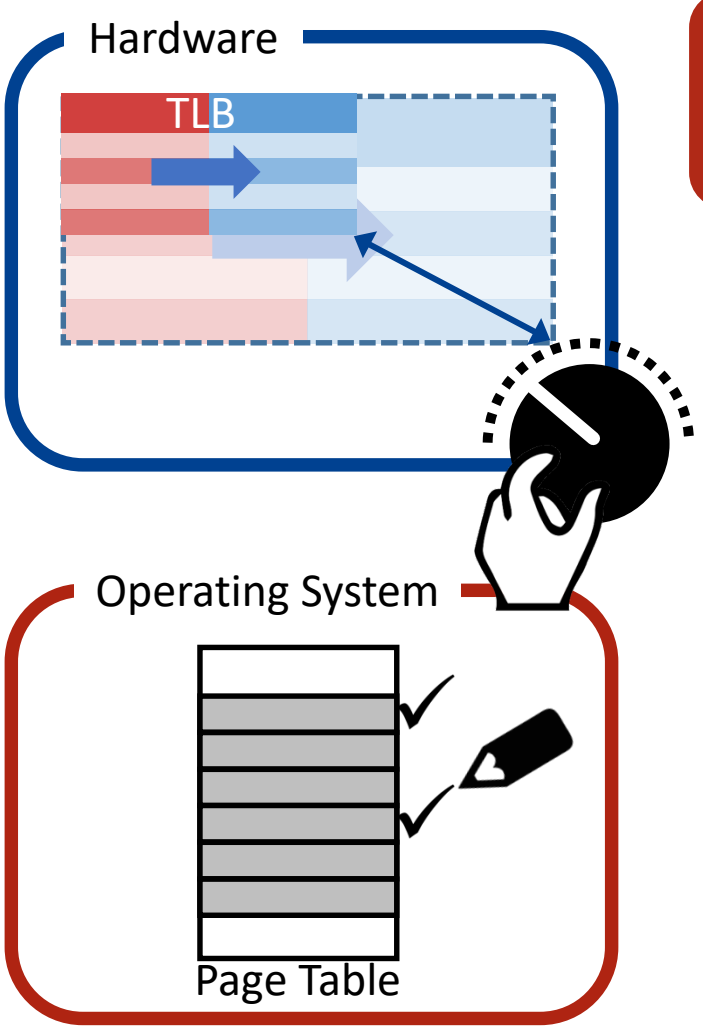

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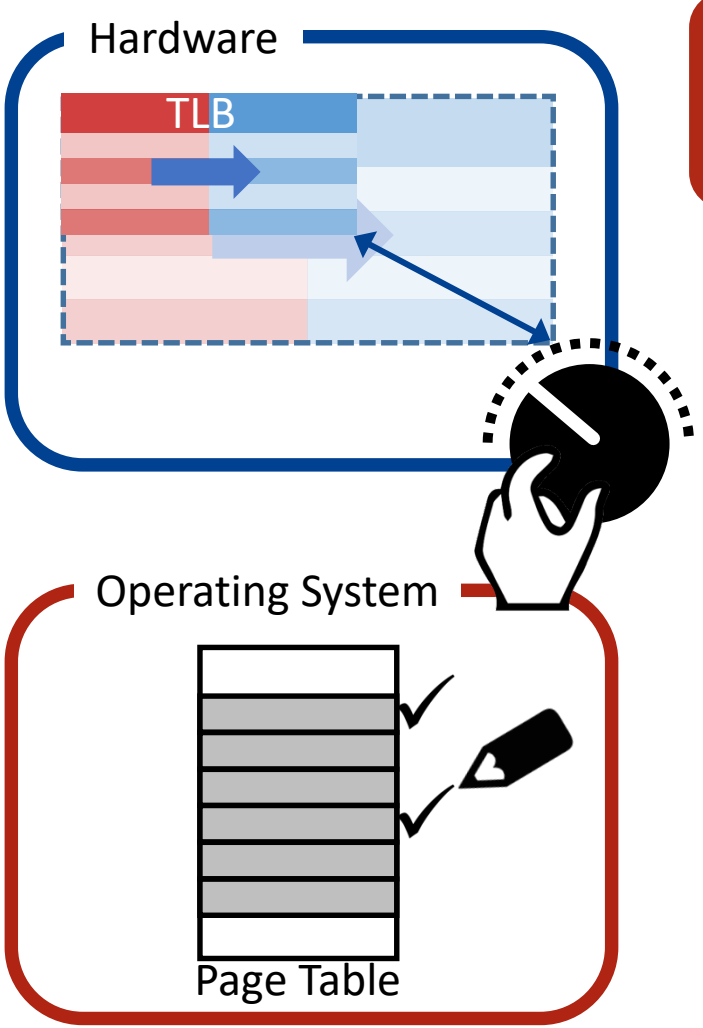

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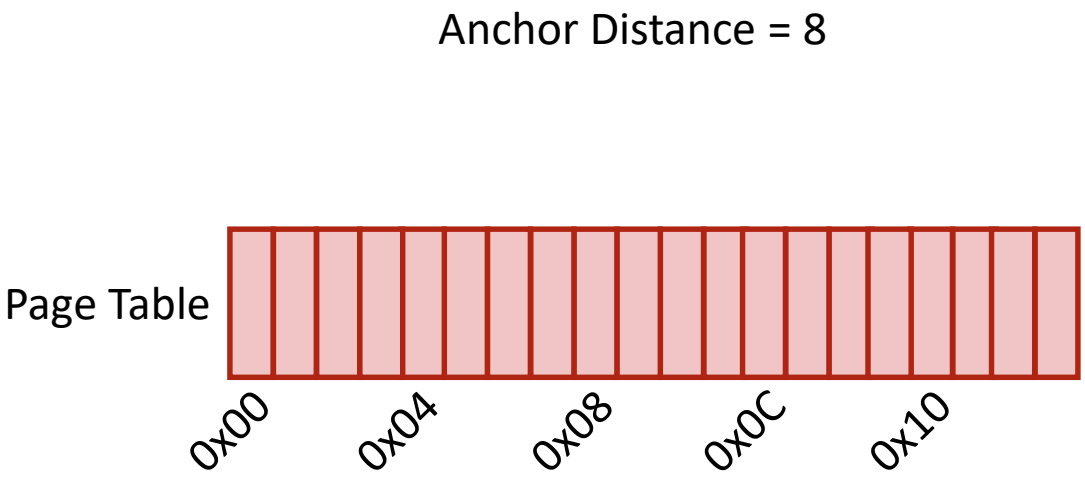

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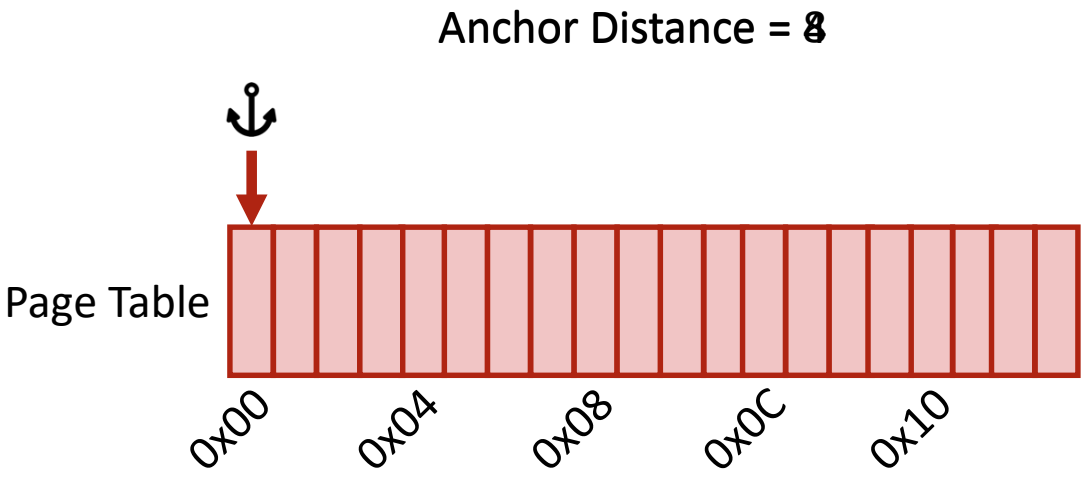

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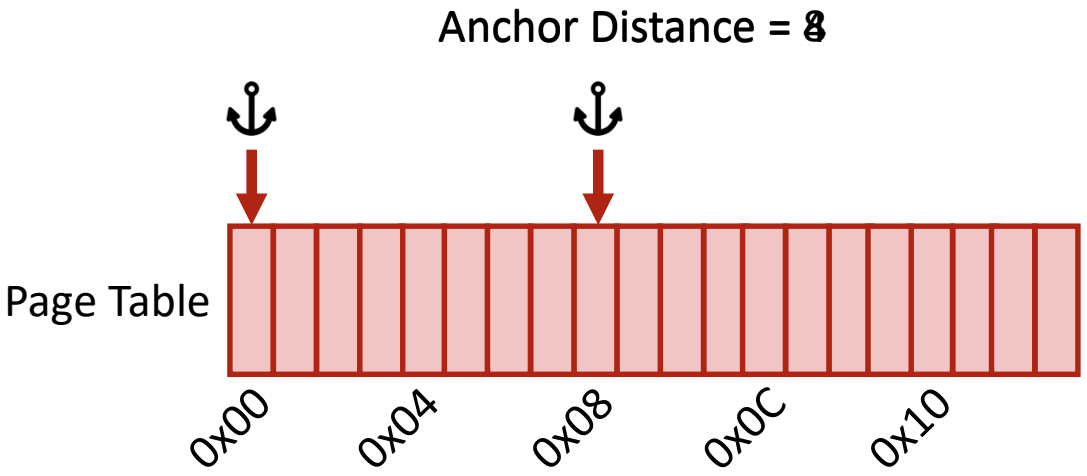

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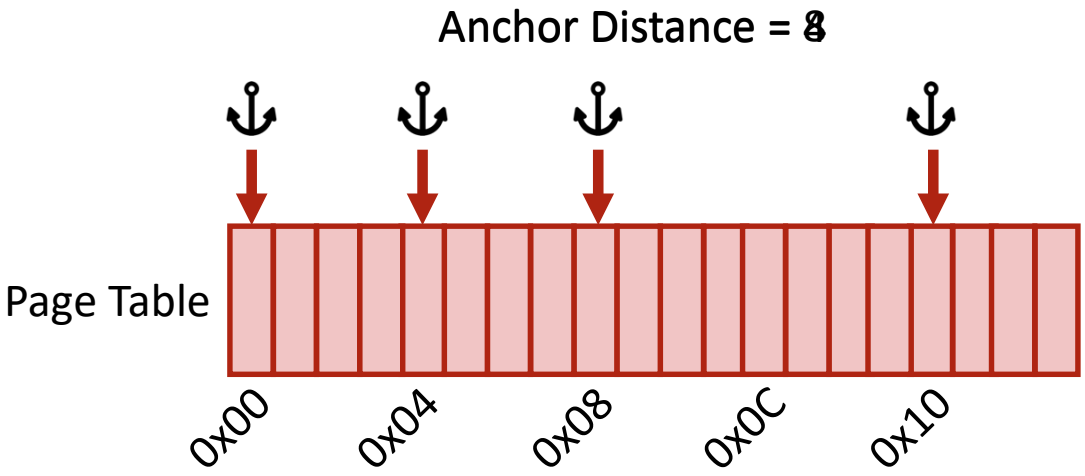

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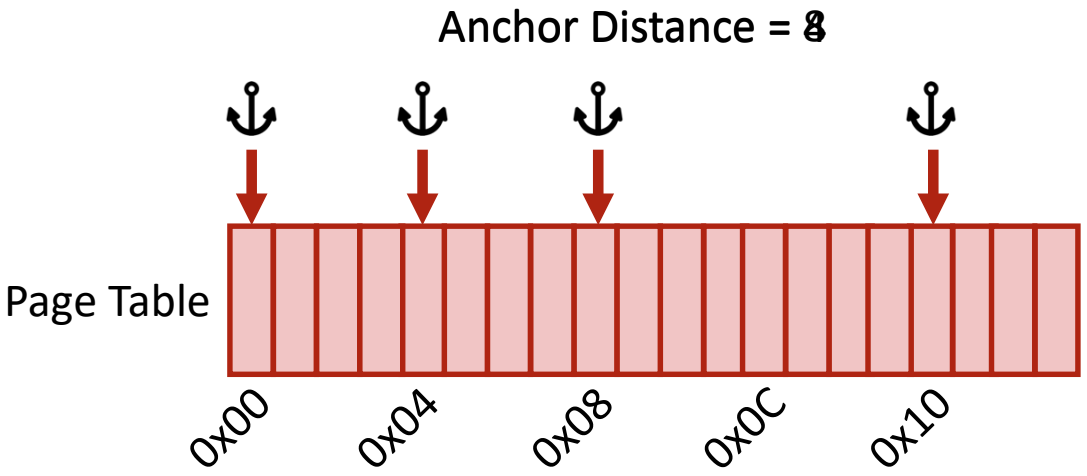

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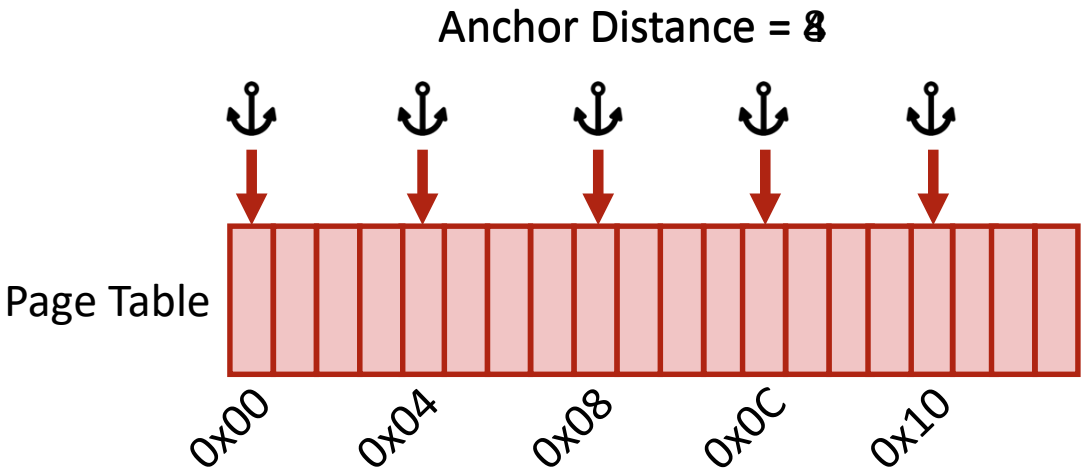

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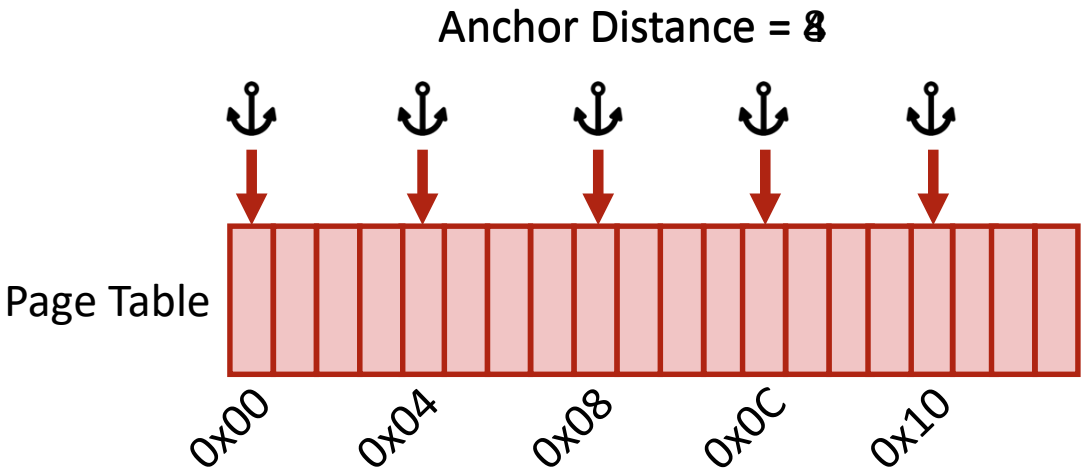
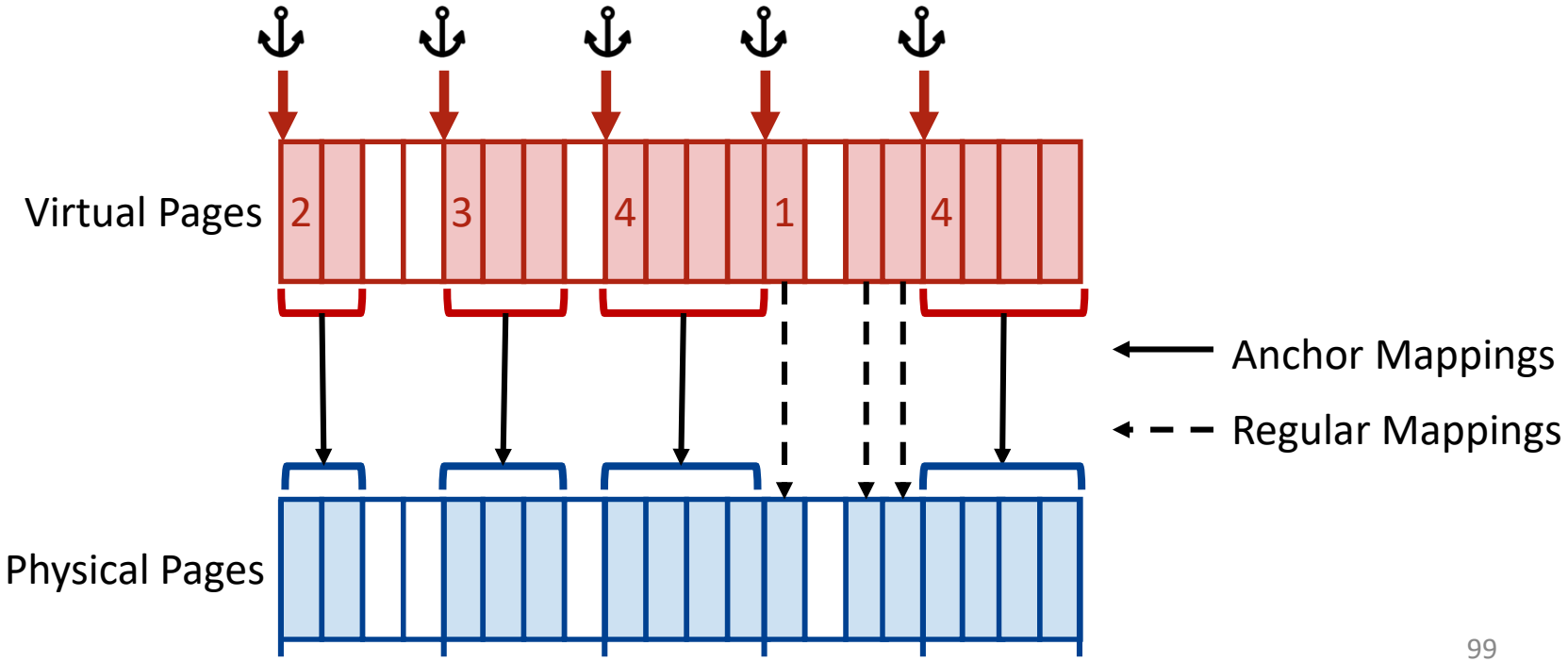
  - Placed at every alignments of anchor distance
  - Anchor distance is a power of 2 (for encoding efficiency)
  - Anchor distance configurable by OS



Anchor Page Table

- Uses the Page Table
- Anchor covers up to distance(4) contiguous pages
  - Each anchor represents contiguity that begins at anchor
- OS marks contiguity onto the anchor page table



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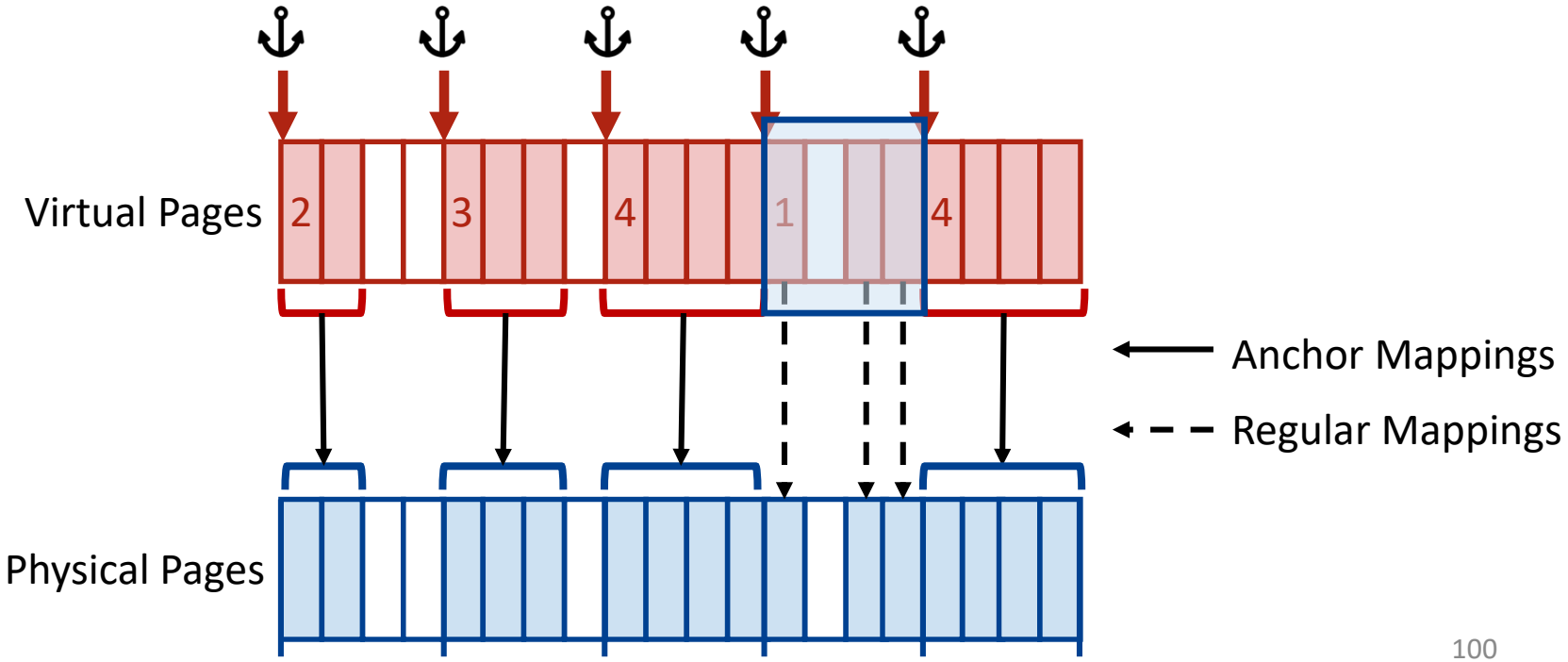

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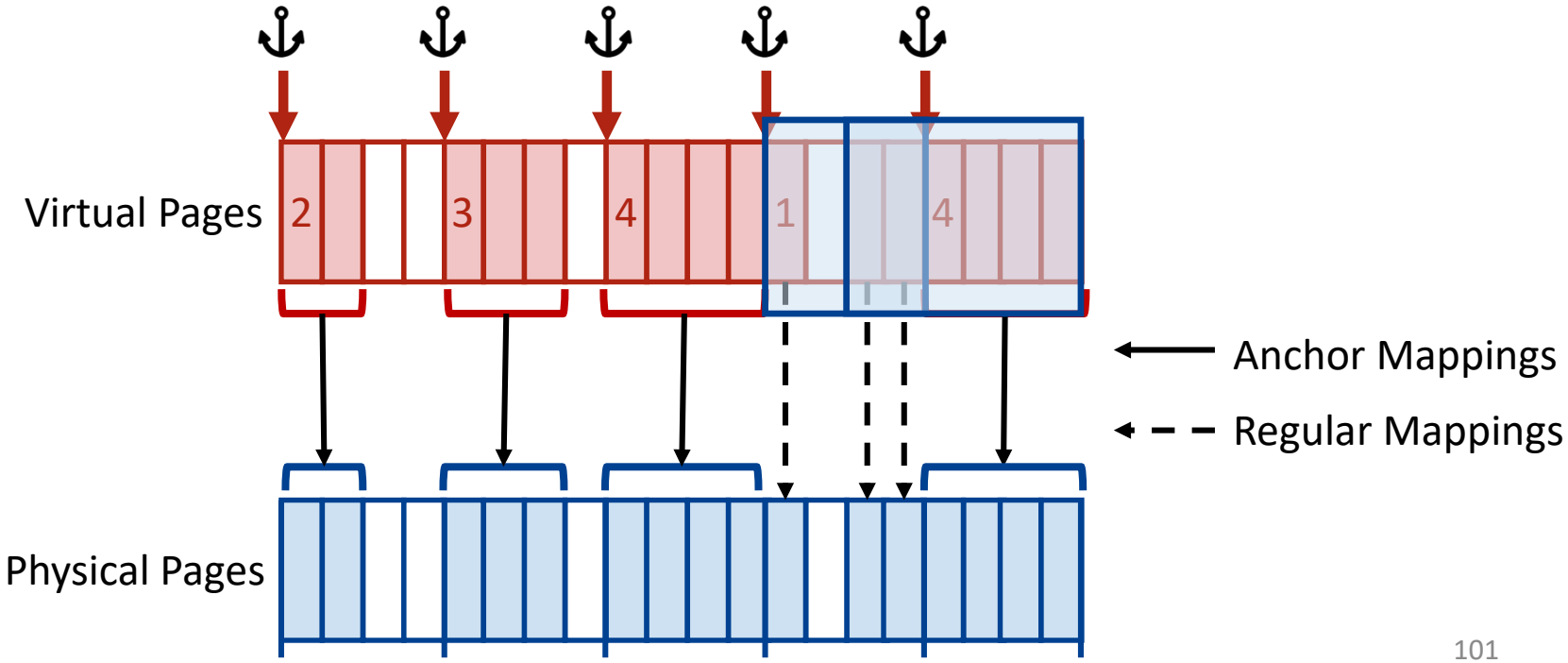
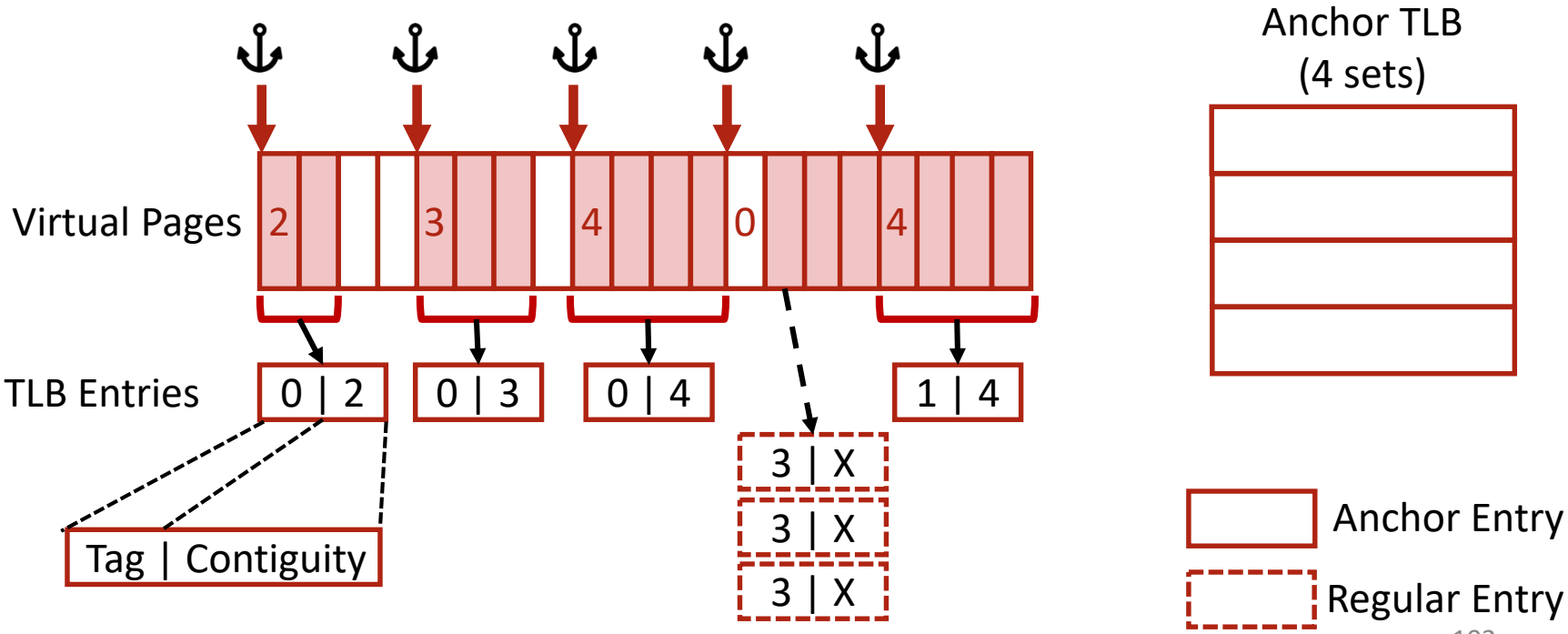


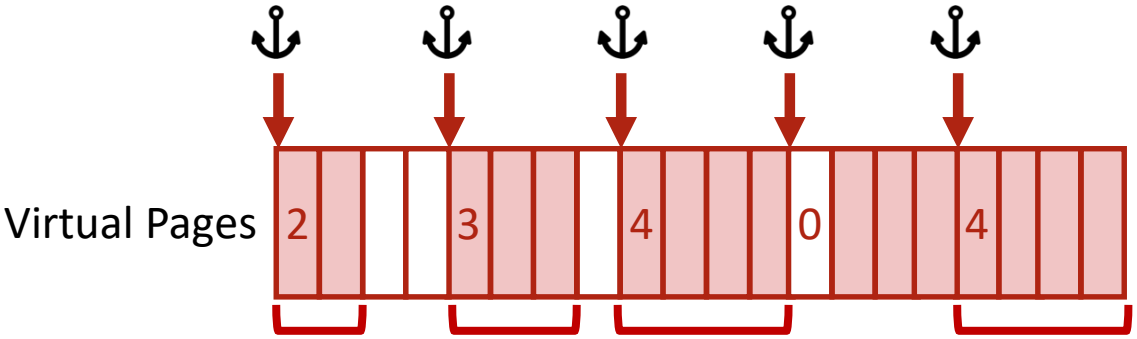
Anchor TLB

- Integrated into the L2 TLB
  - L1 keeps regular entries
- Caches both regular and anchor page table entries
  - Regular and anchor indexed differently



Anchor TLB Lookup

- On L1 TLB Miss Anchor TLB looks up
  - Regular TLB first
  - Anchor TLB next



Anchor TLB
(4 sets)

0 | 2	1 | 4
0 | 3	3 | X
0 | 4	3 | X
3 | X	

Anchor Entry

Regular Entry

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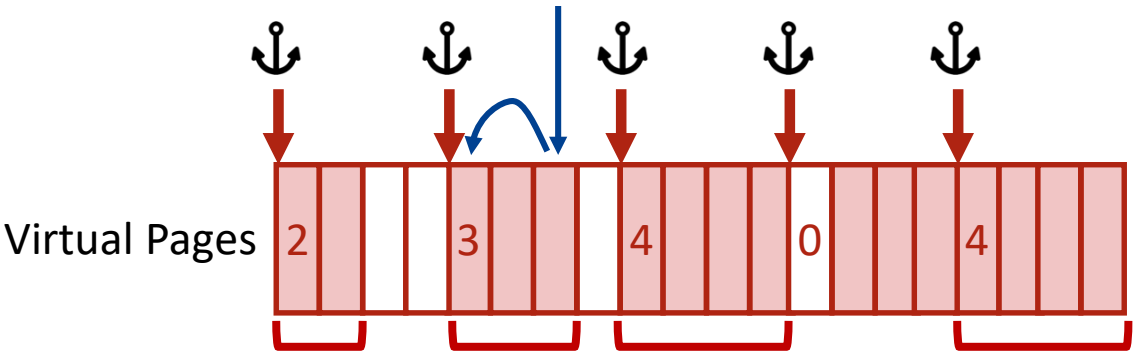

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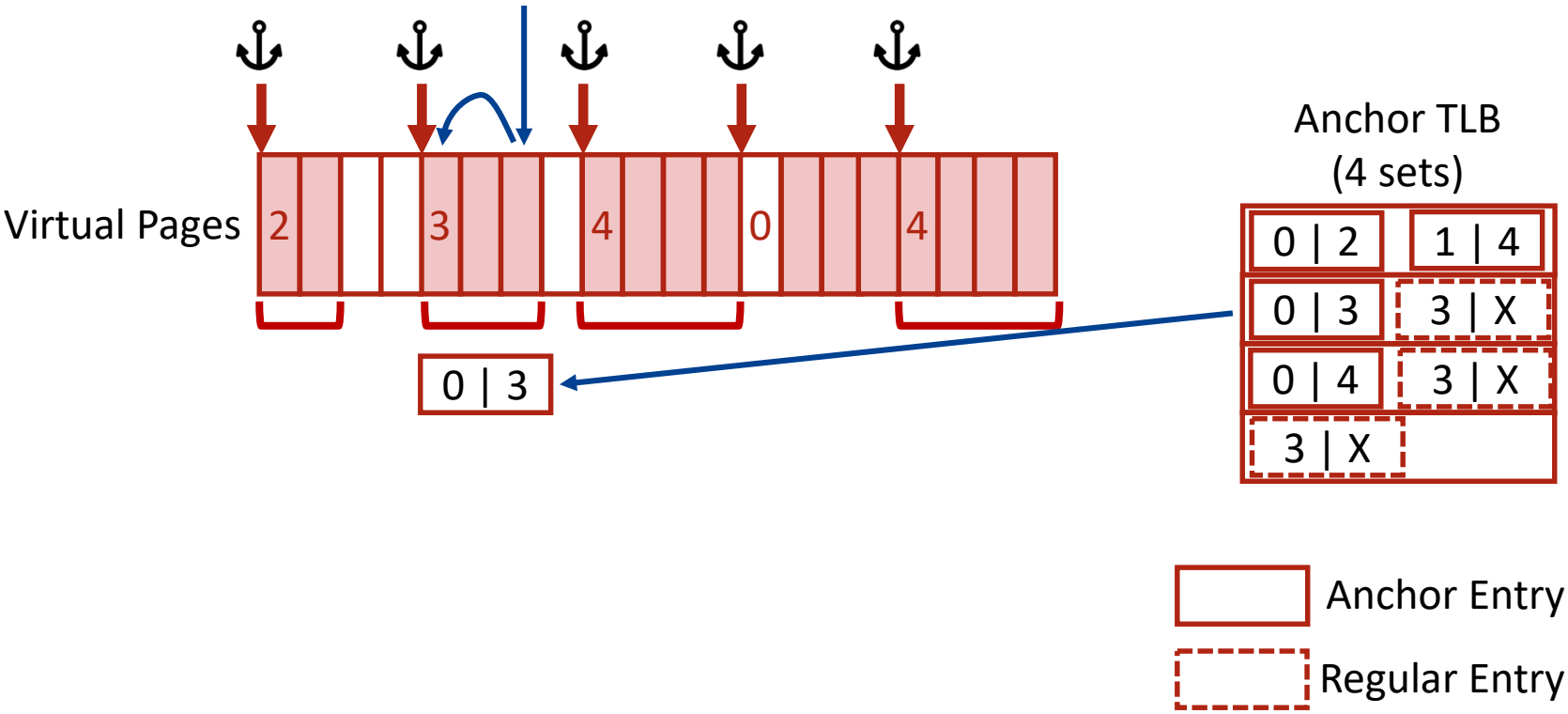

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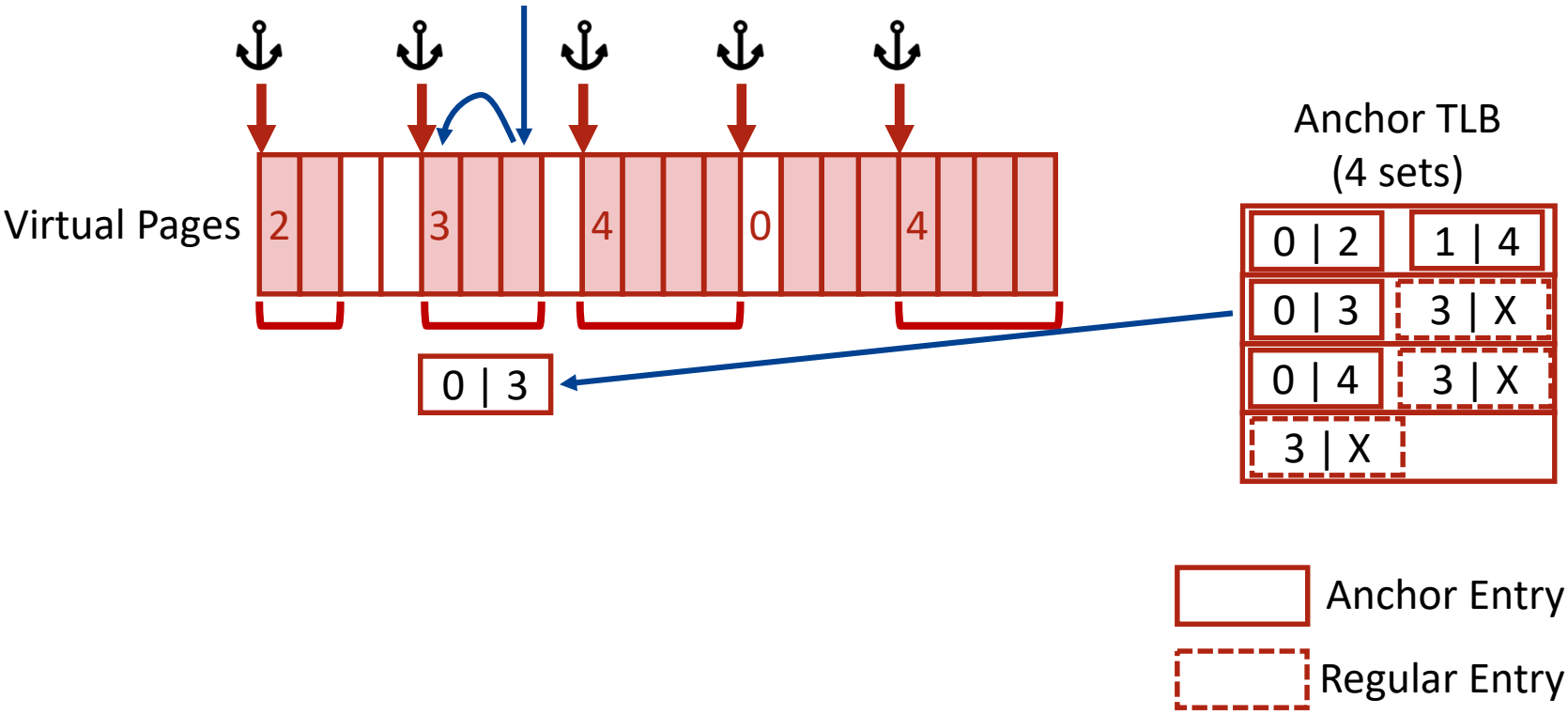

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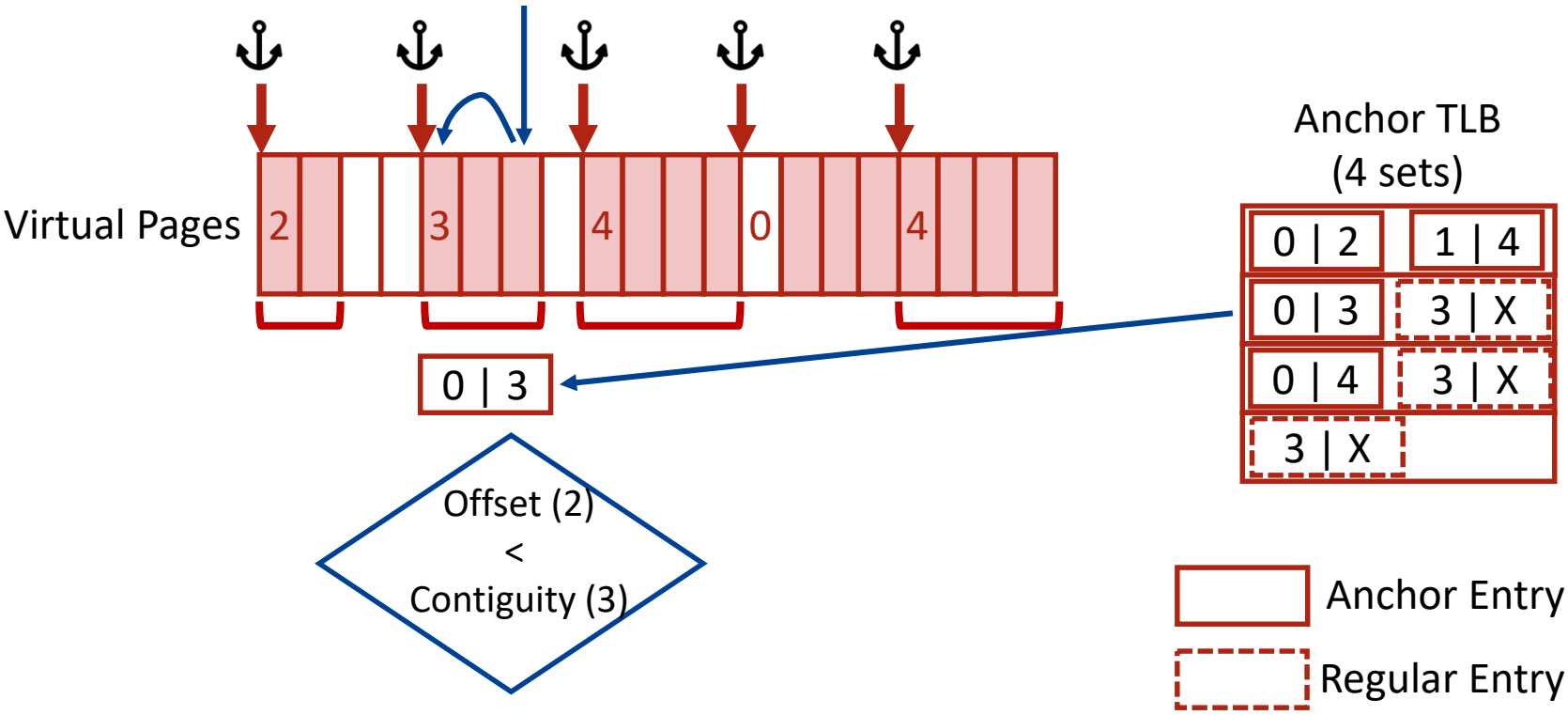

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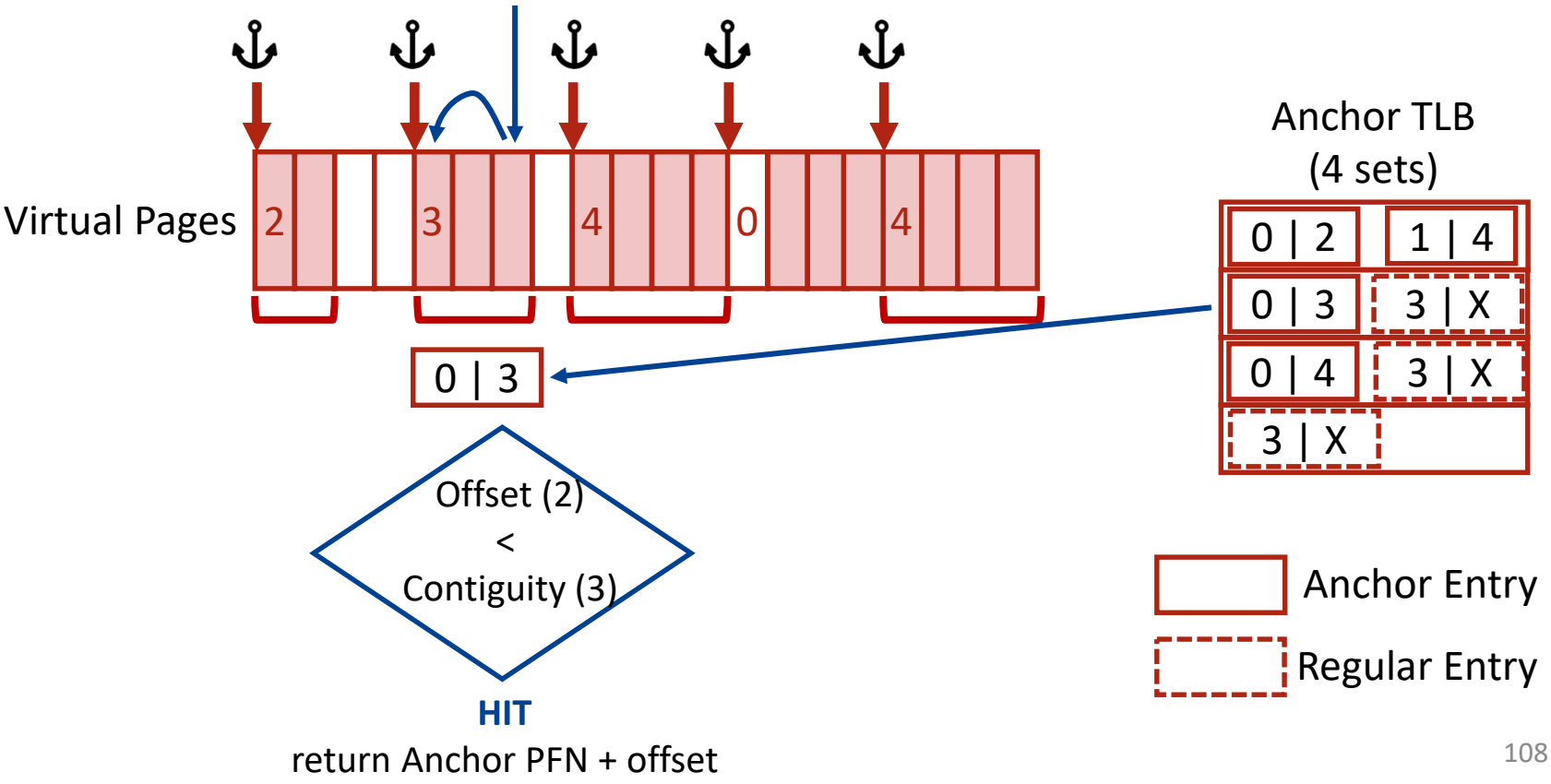

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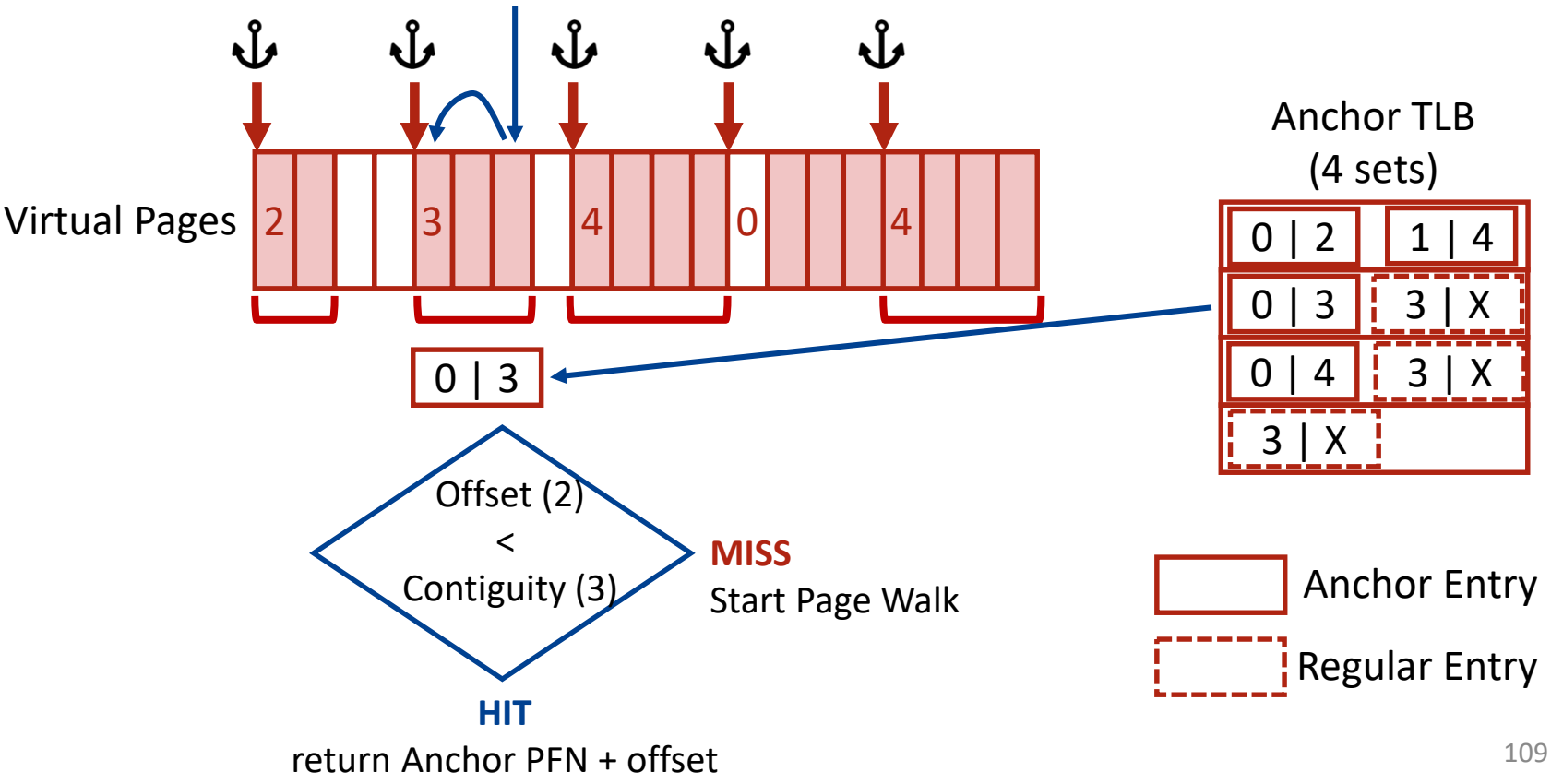

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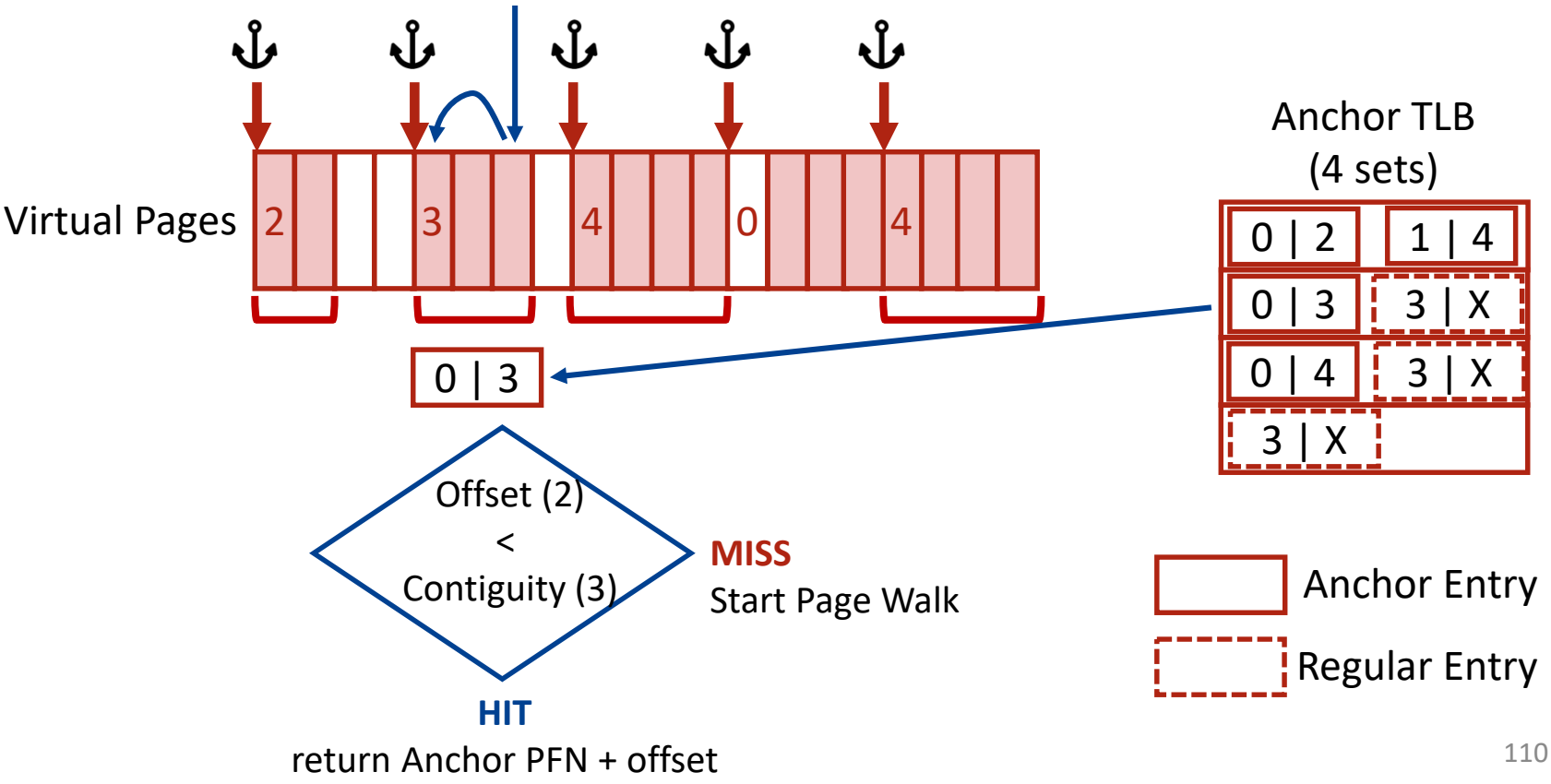


Operating System Responsibilities

- OS periodically selects process anchor distance
  - Heuristic algorithm to minimize TLB entry count
- OS adjusts anchor distance
  - Anchor distance based on selection algorithm
- OS marks mapping contiguity
  - Memory mapping contiguity in anchor page table entry

Simulation Methodology

- Trace based TLB simulator (Based on Intel Haswell)

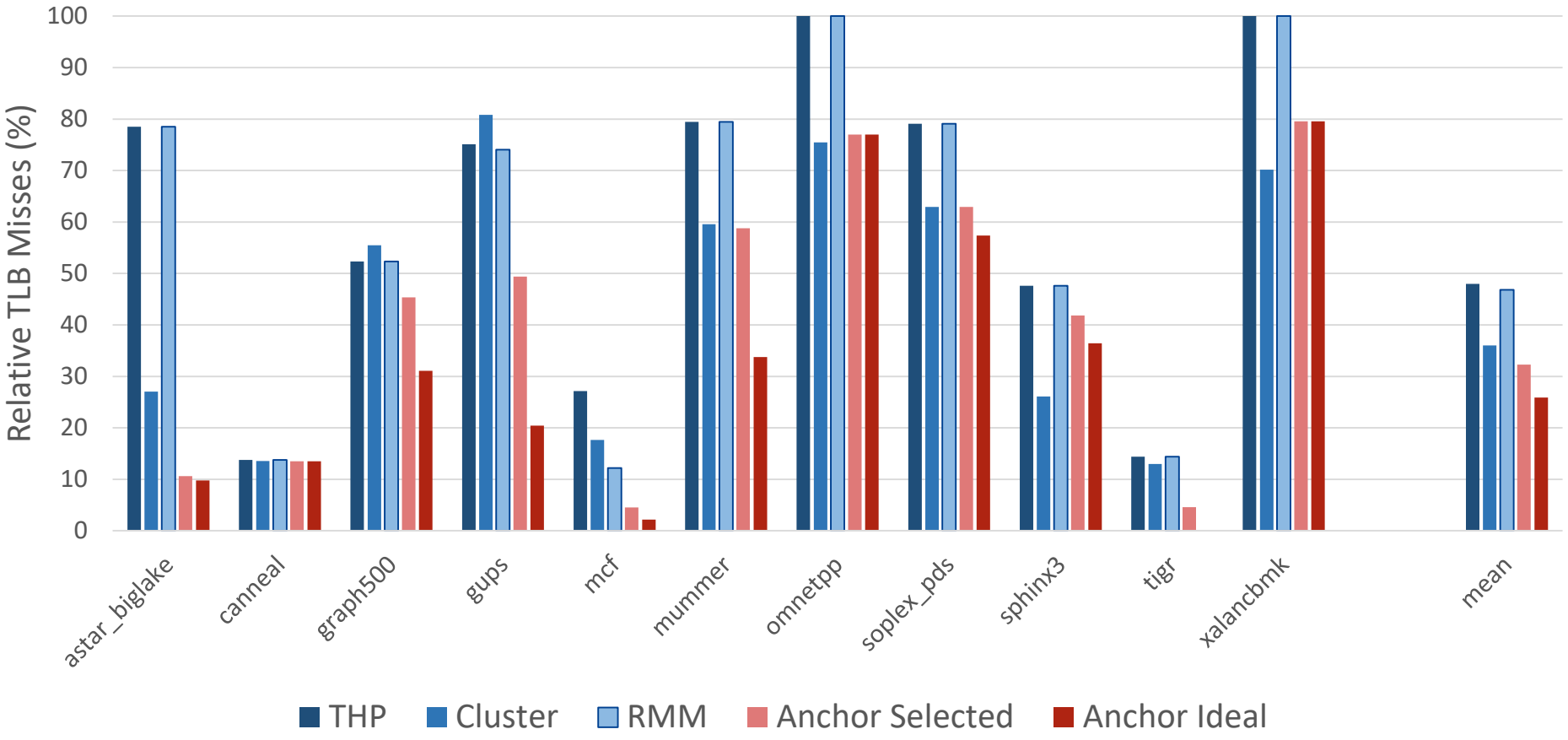
	TLB Configuration	
Common L1	4KB: 2MB:	64 entry, 4 way 32 entry, 4 way
Baseline L2 / THP	4KB/2MB:	1024 entry, 8 way
Cluster	Regular (4KB/2MB): Cluster-8:	768 entry, 6 way 320 entry, 5 way
RMM (Multiple segments)	Baseline L2 TLB + RMM:	 32 entry, fully-assoc.
Anchor (Selected/Static Ideal)	4KB/2MB/anchor:	1024 entry, 8 way

Memory Mapping Scenarios

- Two class of memory mapping scenarios
  - Two real system memory mappings
  - Four synthetic memory mappings

Name	Trace information
demand	Default Linux memory mapping
eager	‘Eager’ allocation
low	1– 16 pages (4KB – 64KB)
medium	1 – 512 pages (4KB – 2MB)
high	512 – 64K pages (2MB – 256MB)
max	Maximum contiguity

Evaluation – TLB Misses of demand **mapping**



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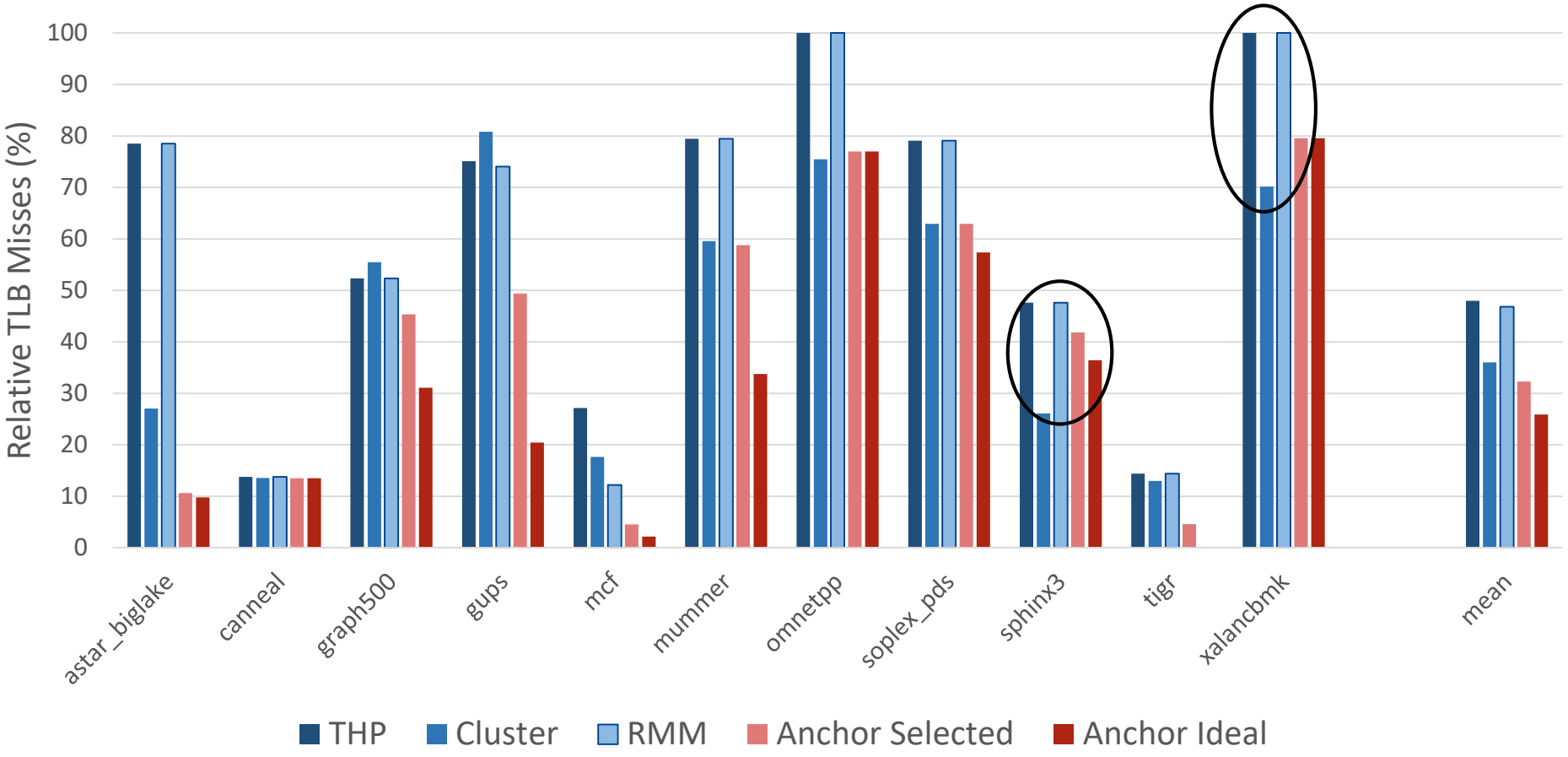

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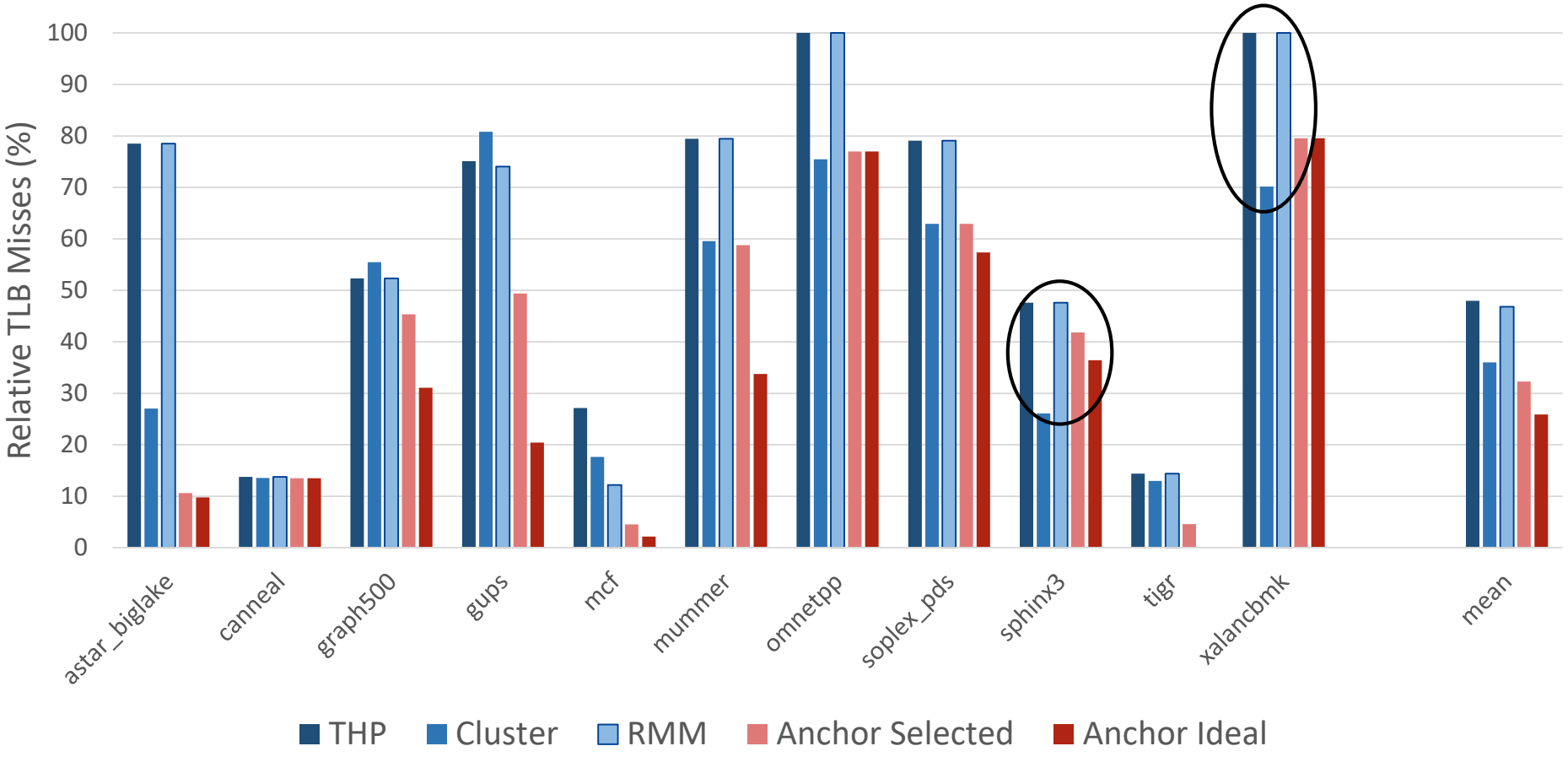

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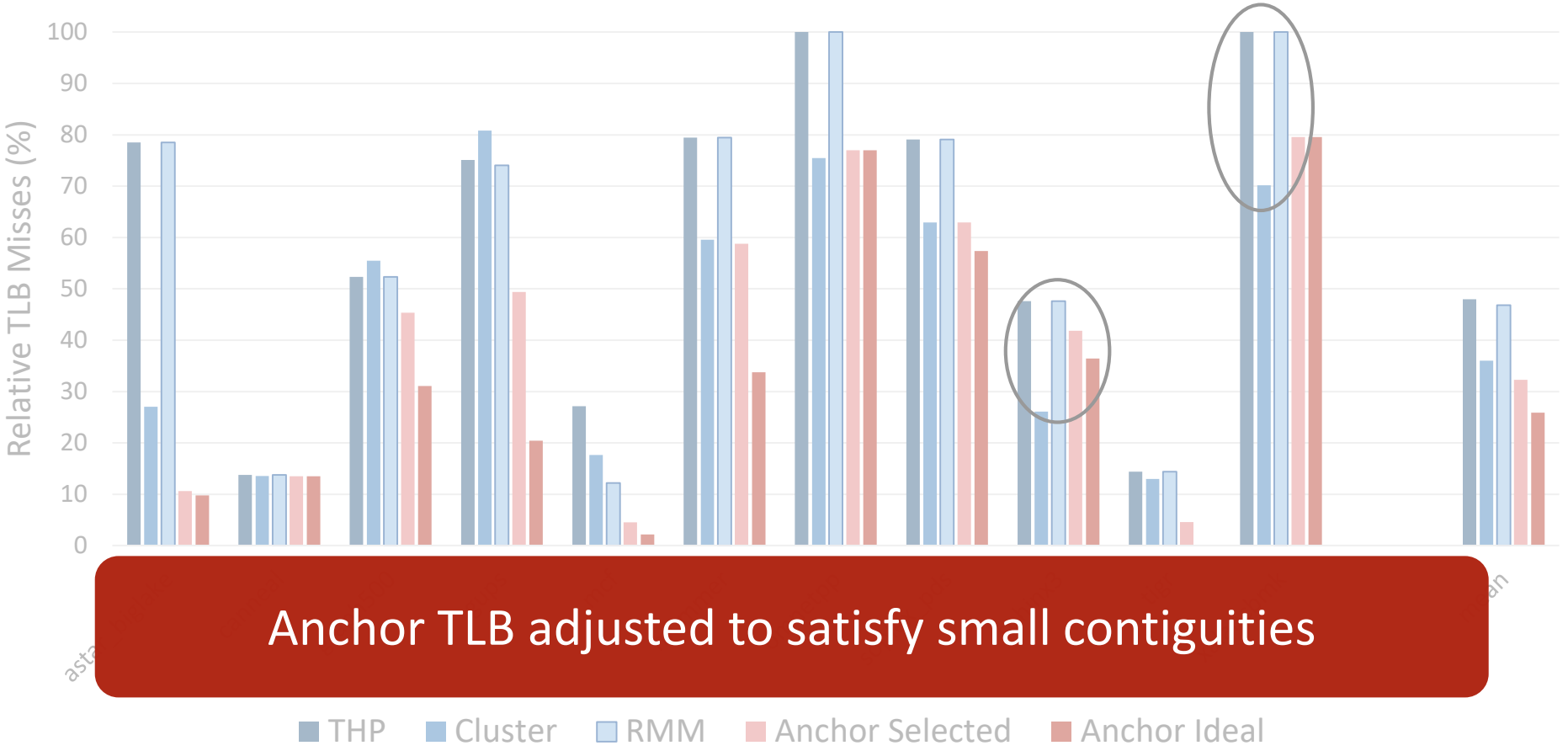
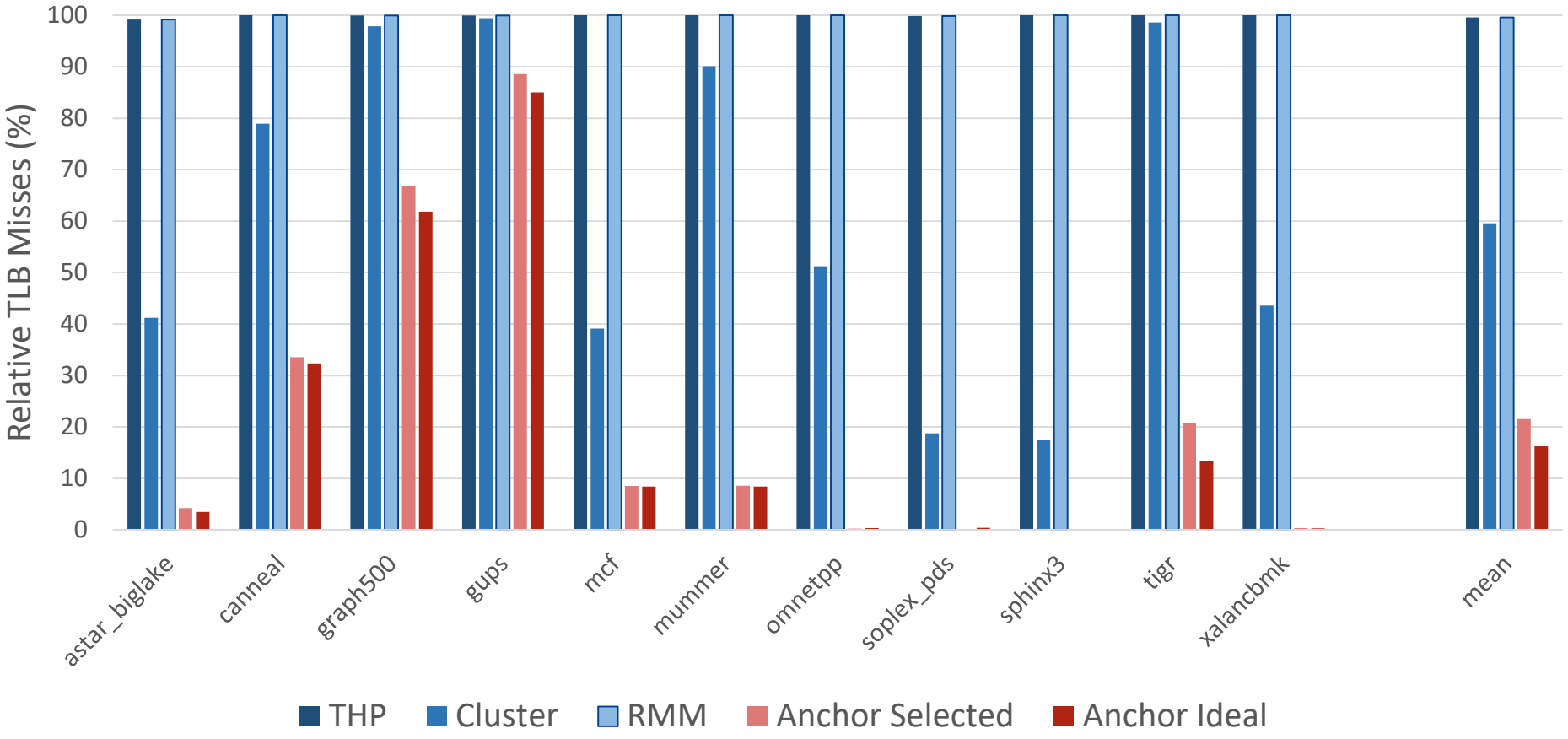
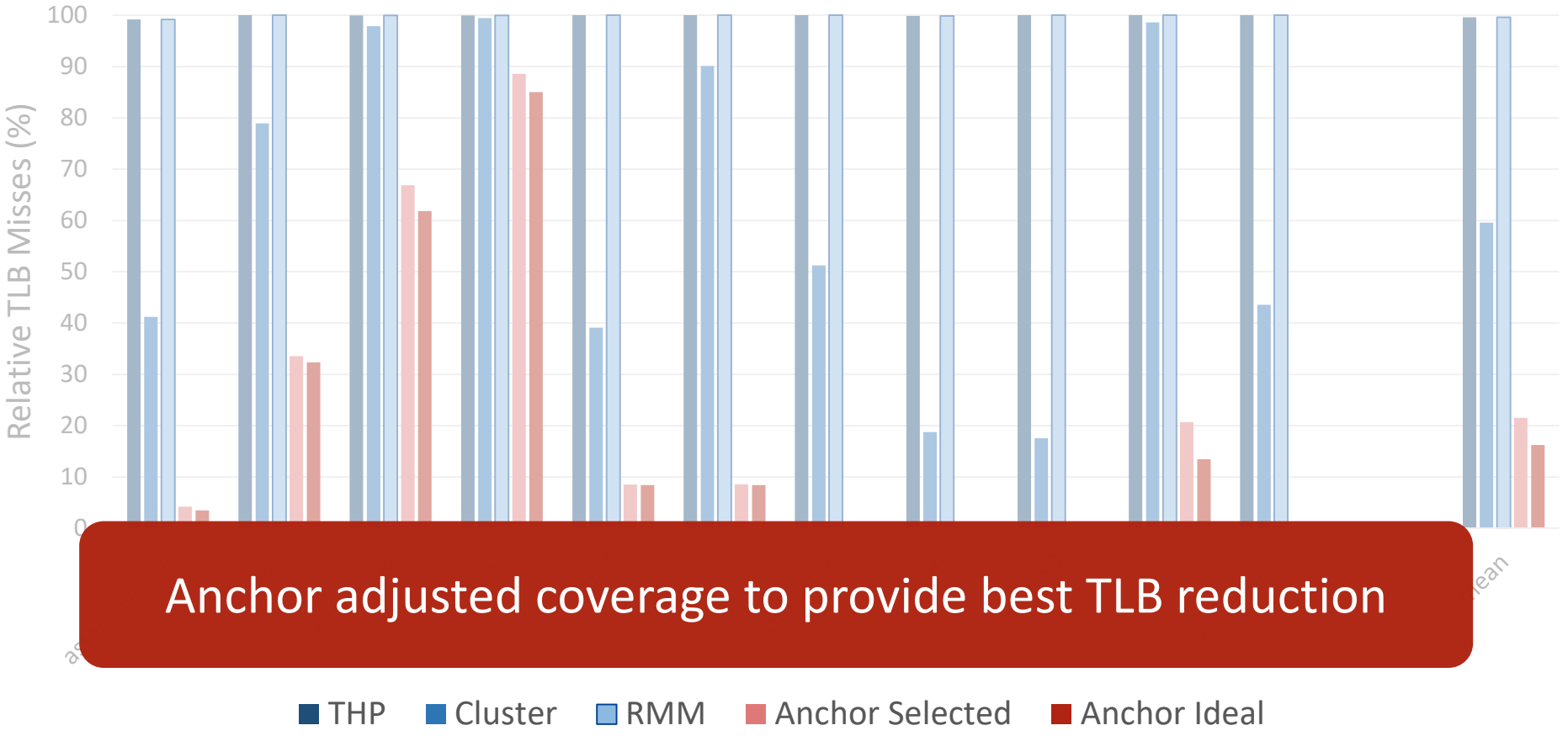


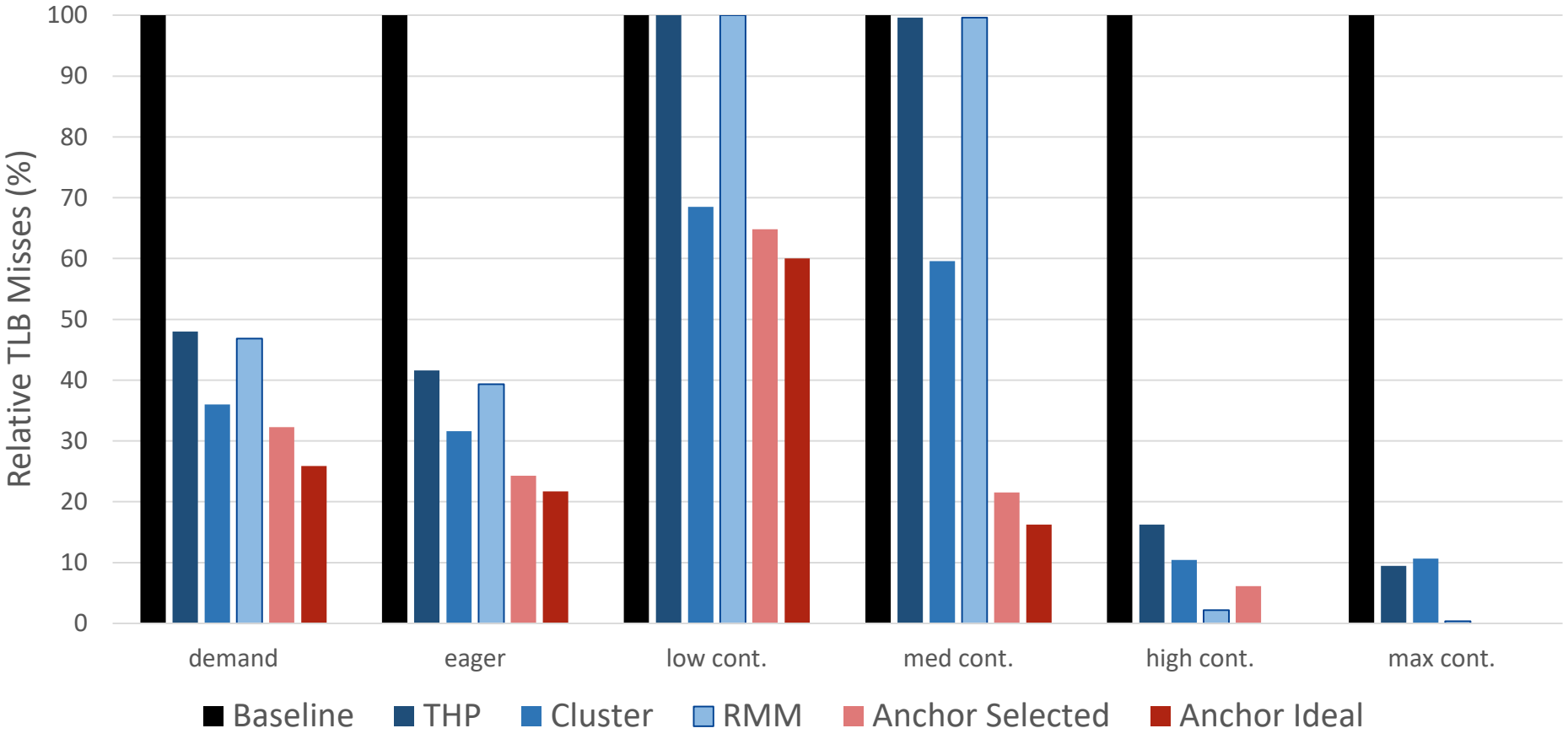
Evaluation – TLB Misses of medium **mapping**



Evaluation – TLB Misses of medium **mapping**



Evaluation – TLB Misses of all mapping



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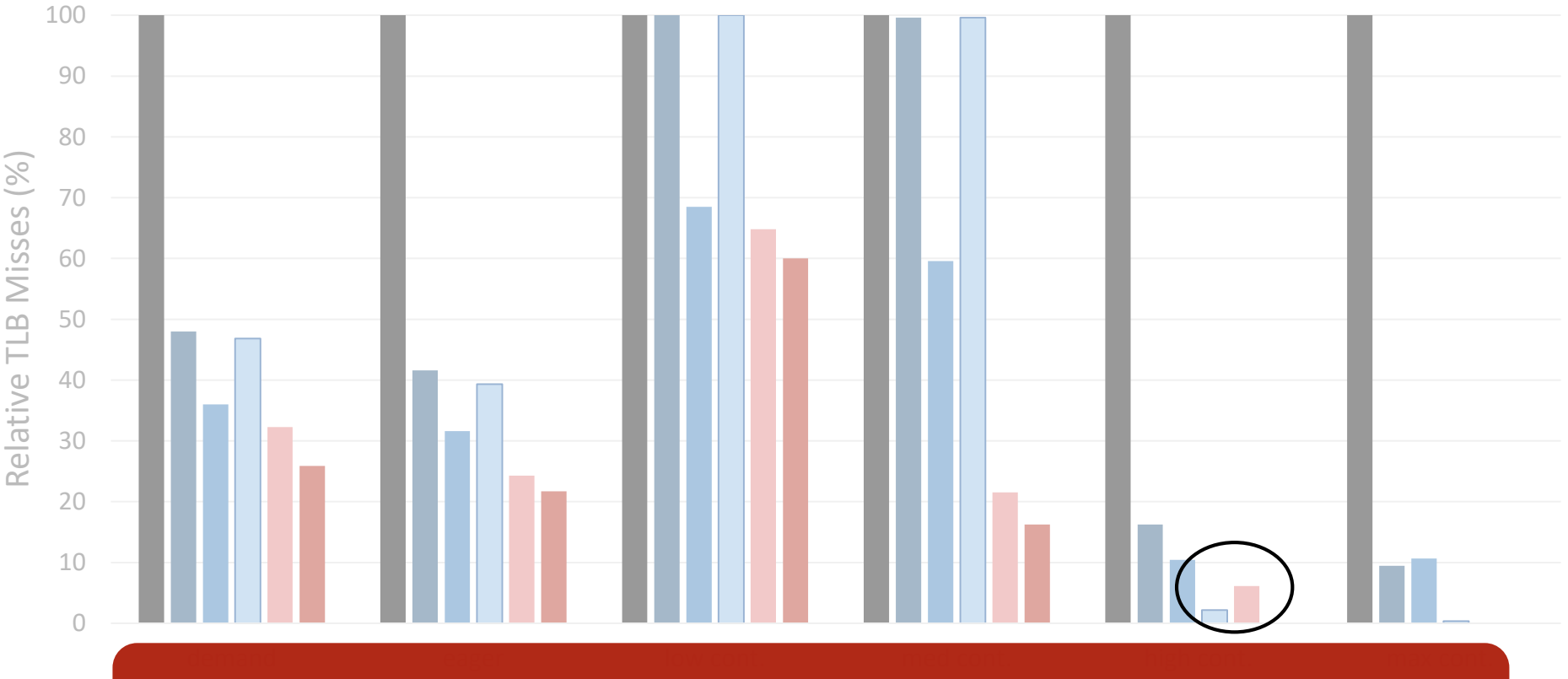

Anchor TLB performs well for diverse mapping scenarios

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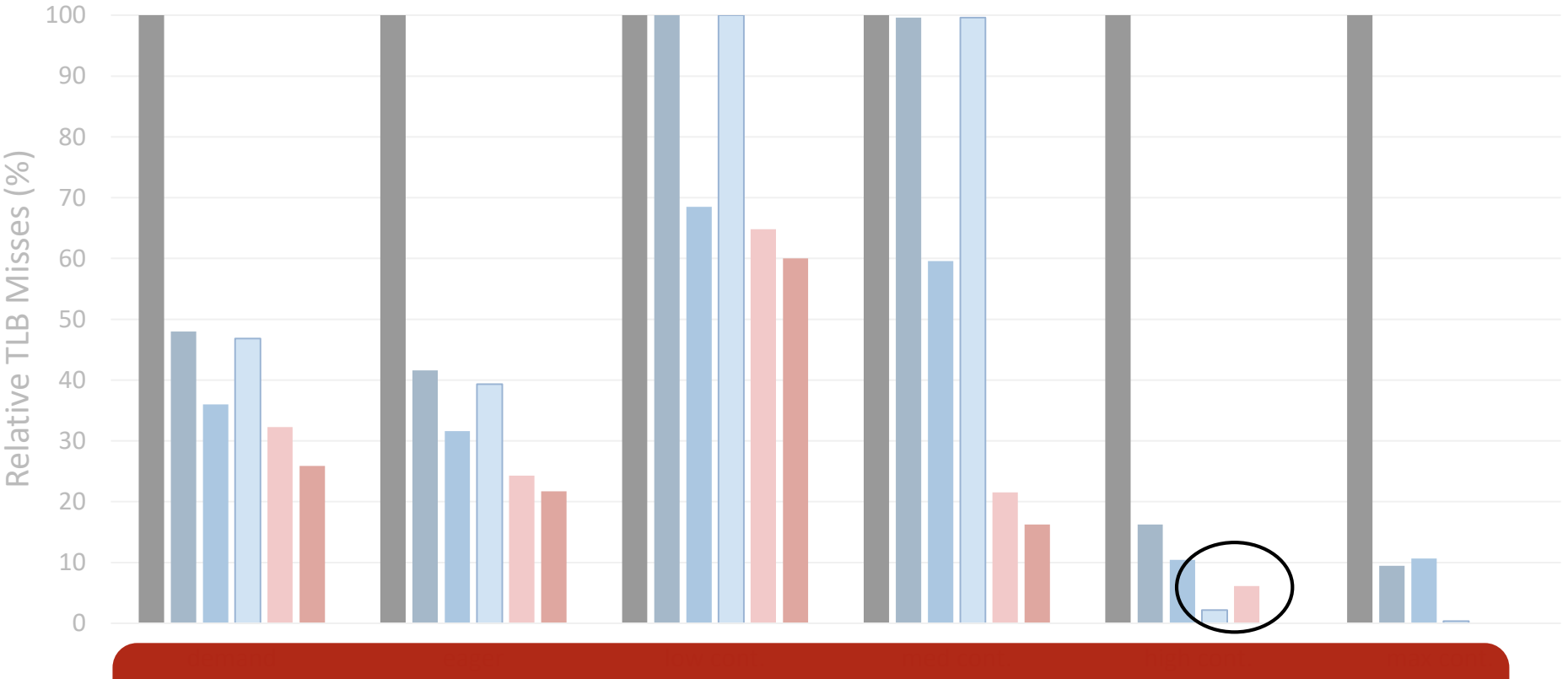

Anchor TLB performs well for diverse mapping scenarios

Conclusion

- Hybrid TLB Coalescing is a HW-SW joint effort
- Anchor TLB provides adjustable coverage
  - TLB entry coverage grows and shrinks dynamically
- OS provides contiguity hint using the page table
- OS picks adequate contiguity per-process

- Hybrid TLB Coalesce performs:
  - Best for Small-Intermediate contiguities
  - Similar to best prior scheme for Large contiguities