Heterogeneous Isolated Execution for Commodity GPUs

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Heterogeneous computing is emerging (GPUs, FPGAs, etc)



Machine Learning

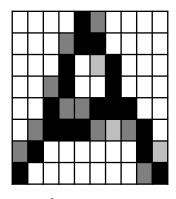


Image Processing

$$\int \frac{dy}{dx}$$

Complex Calculations

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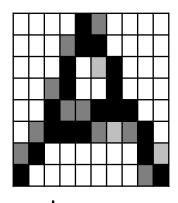


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Untrusted Kernel Space

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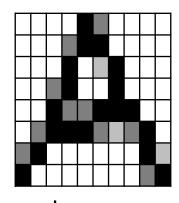


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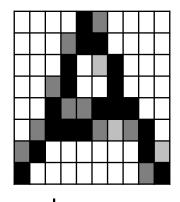


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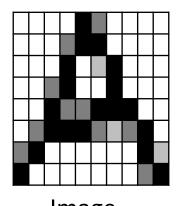
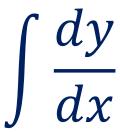
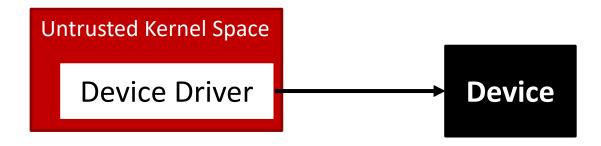


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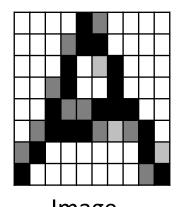
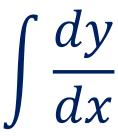
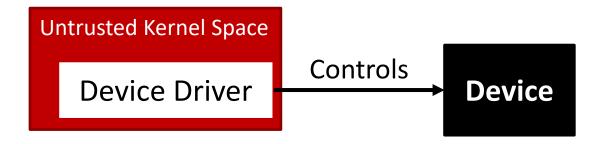


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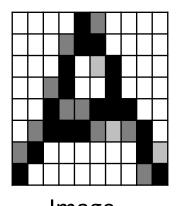
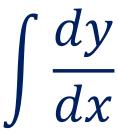


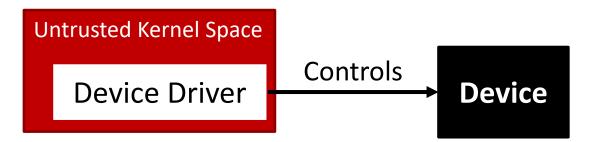
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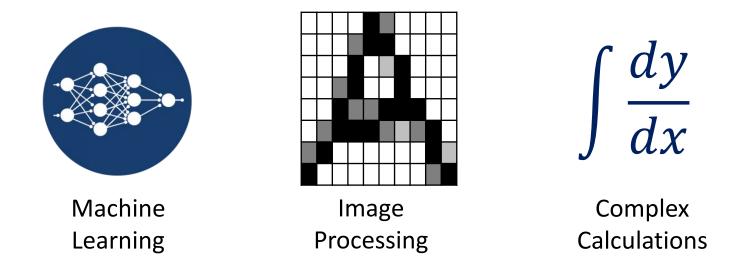
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User

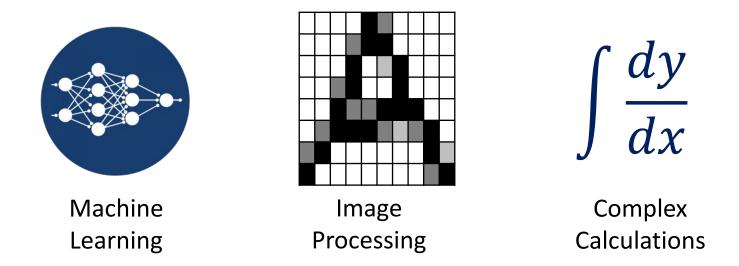


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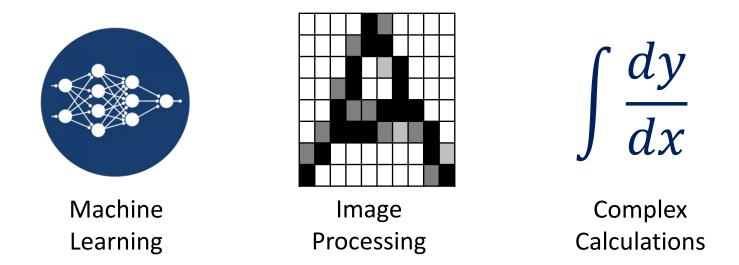


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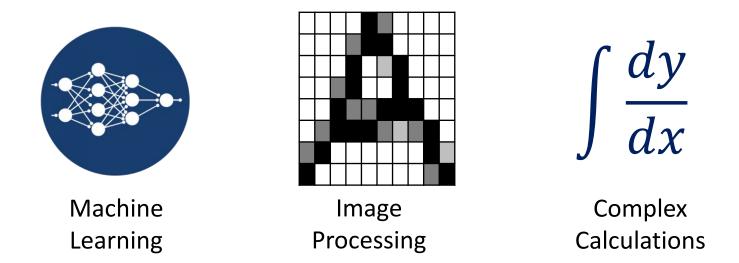


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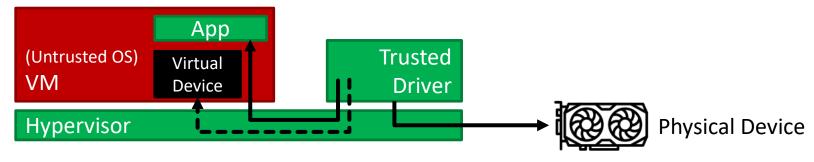




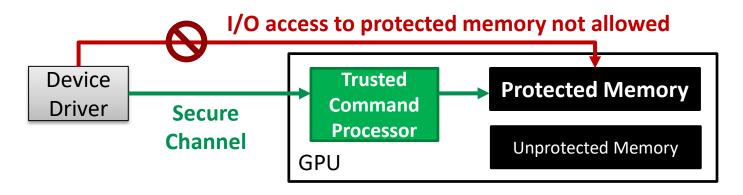
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 - SGXIO [Weiser, CODASPY'17]: use a trusted hypervisor

- Graviton [Volos, OSDI'18]: use a modified GPU with a root of trust

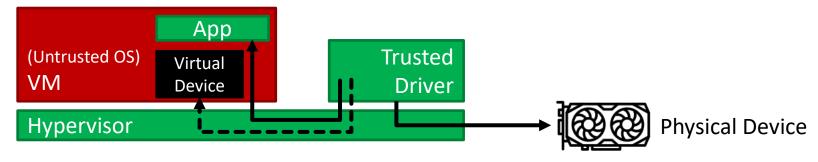
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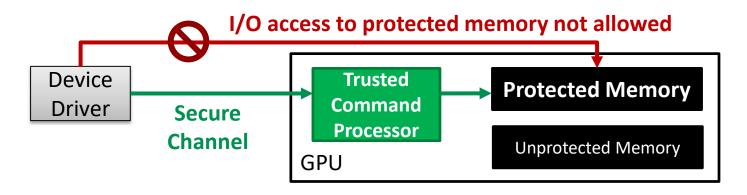
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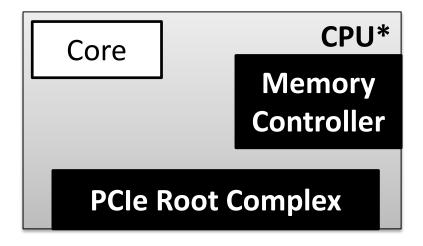


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All device I/O accesses from software are handled by CPU

Process



DRAM

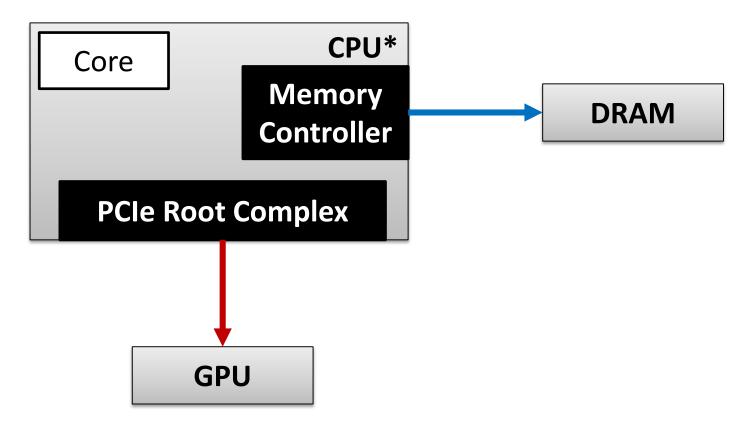
GPU





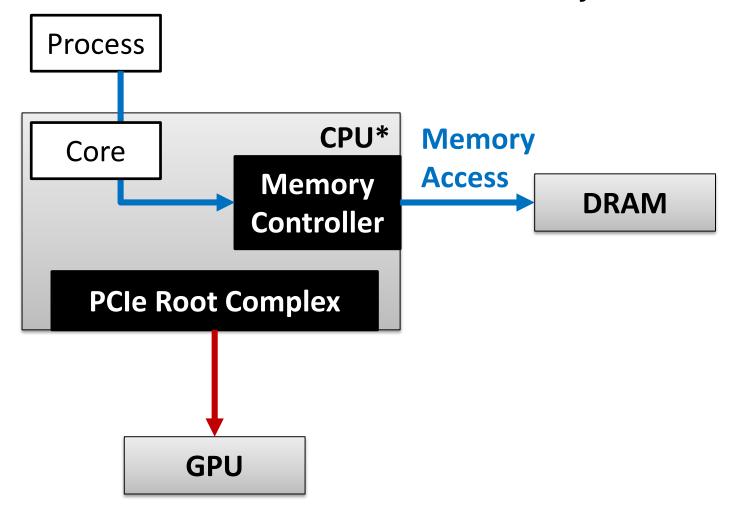
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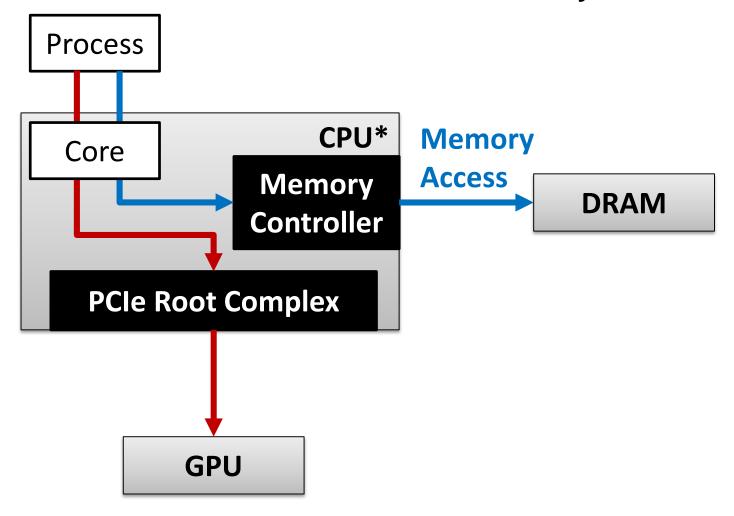
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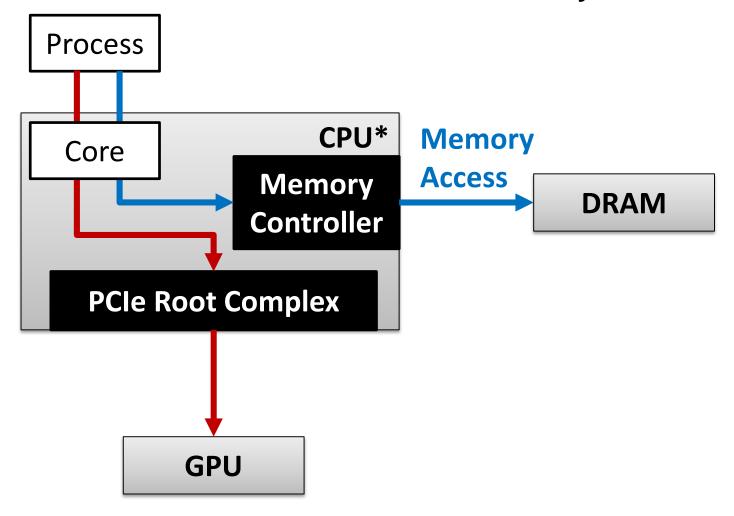


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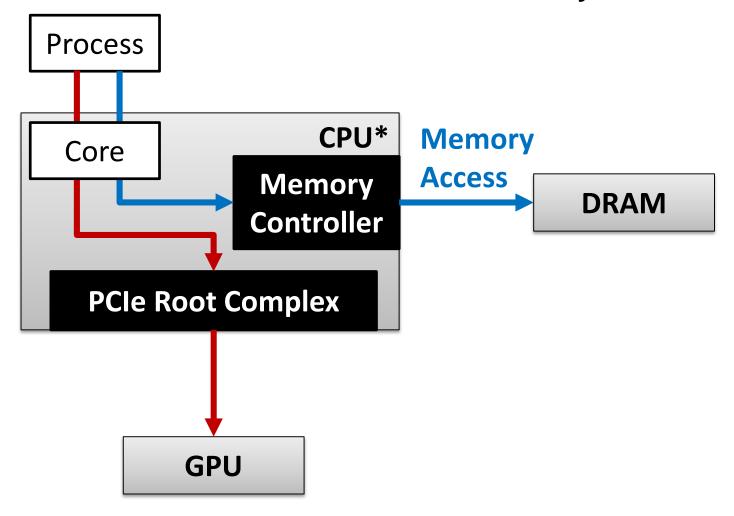


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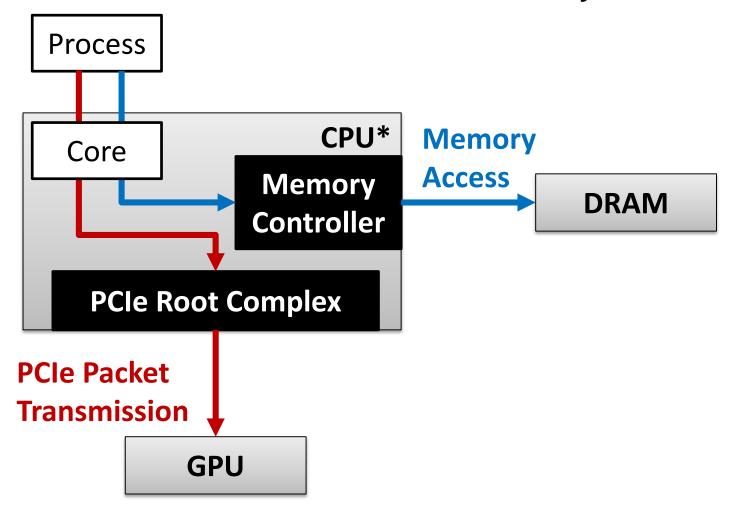


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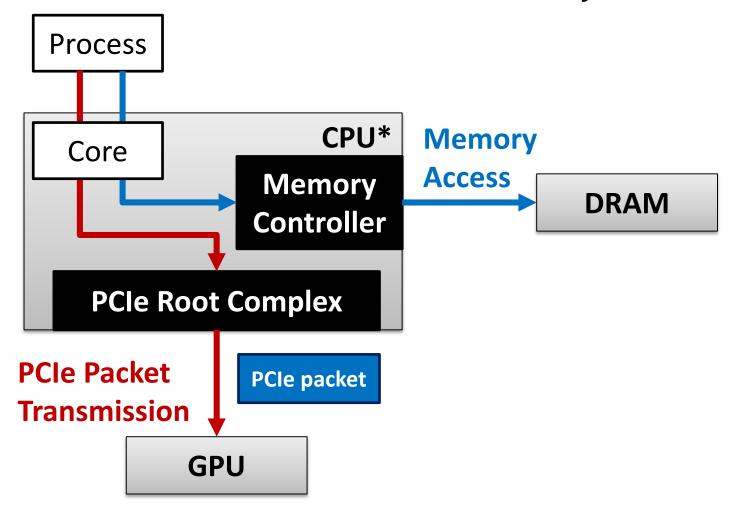
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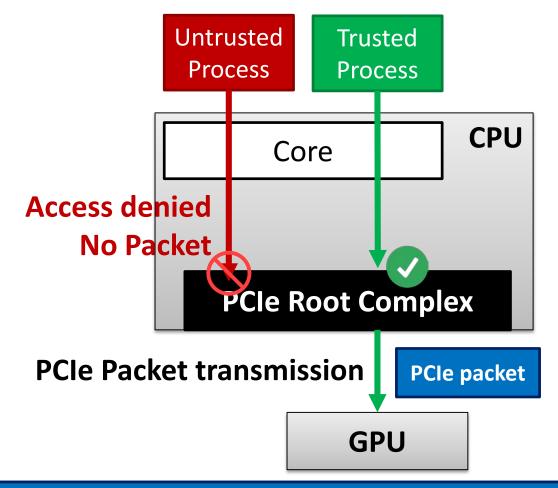
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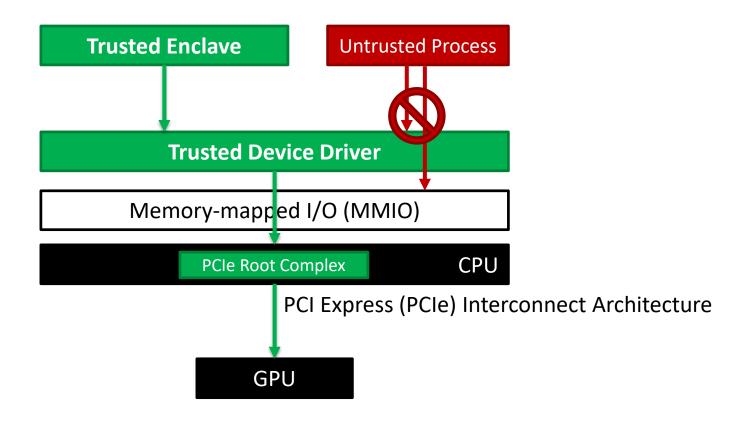




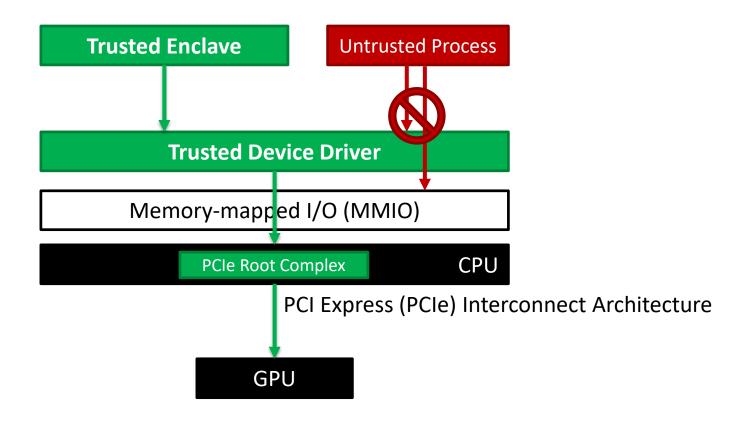
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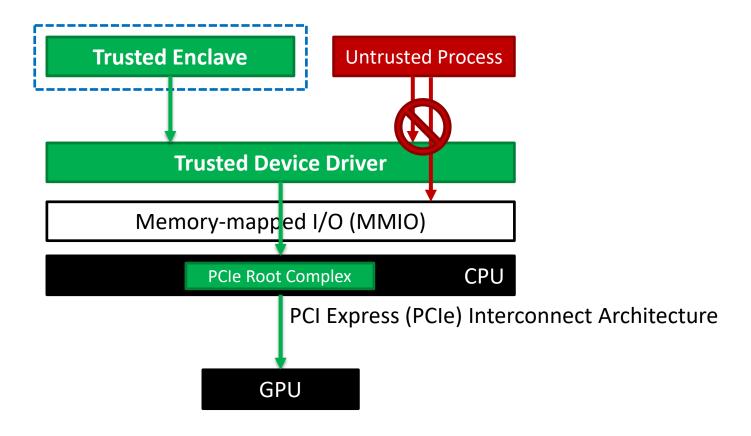
Idea: Prevent I/O from Attackers by Securing I/O Path!



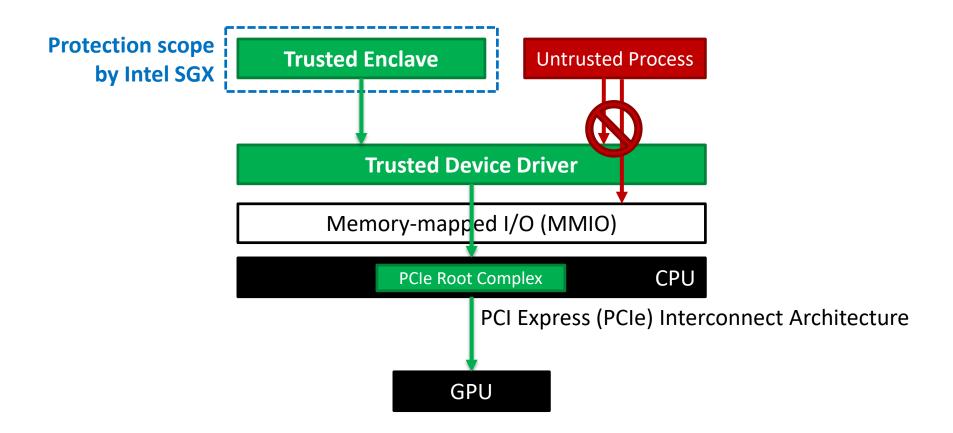
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- Extend TEE to I/O path (from SGX enclave to the device)



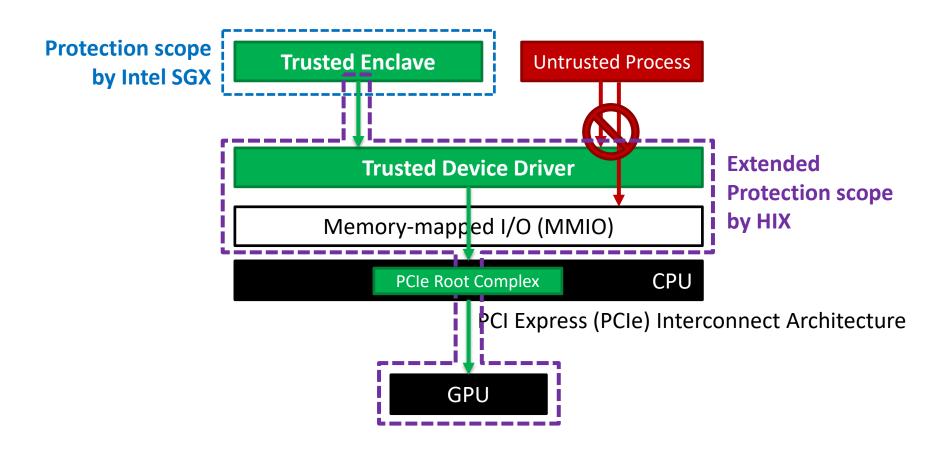
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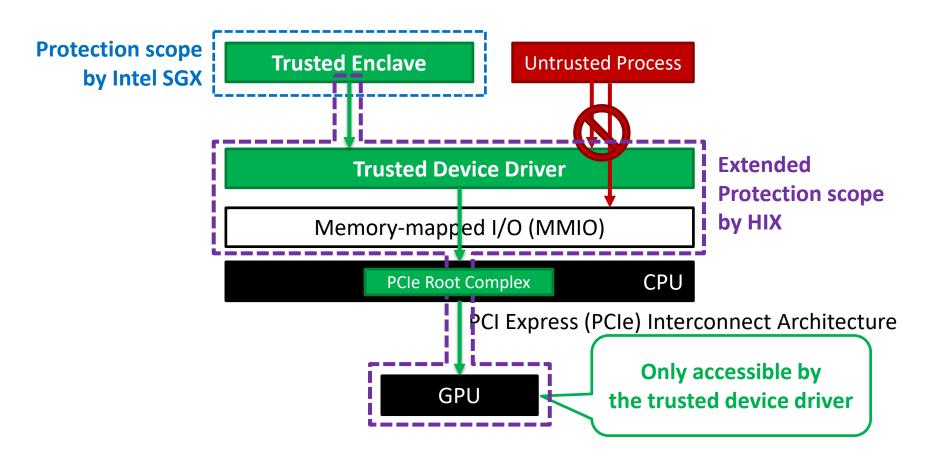
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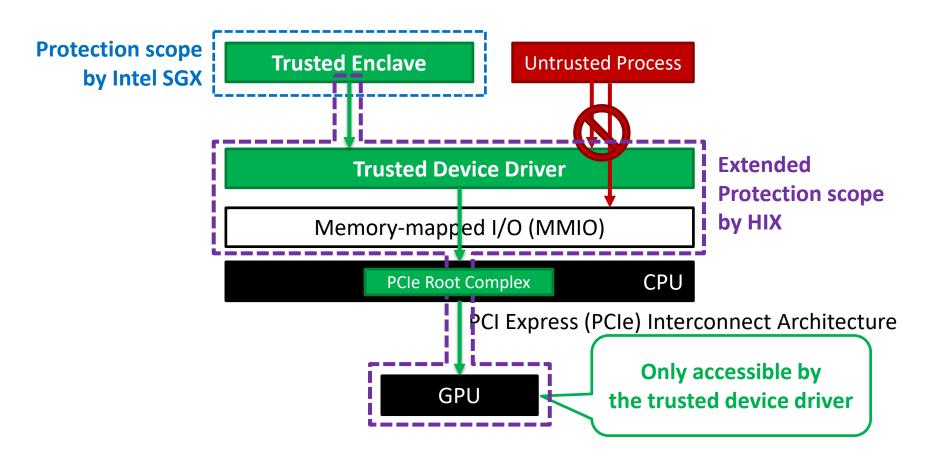
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Contributions and Threat Model



Contributions and Threat Model

- Provide confidentiality and integrity to user data in GPU
- No GPU modifications are required
 - Provide GPU TEE by securing I/O path
 - No protection against physical attacks; software based attacks prevented

Threat Model

- Attackers have all privileged permission on software level
- Not consider physical attacks on any hardware
- Protect the system from privileged software attacks

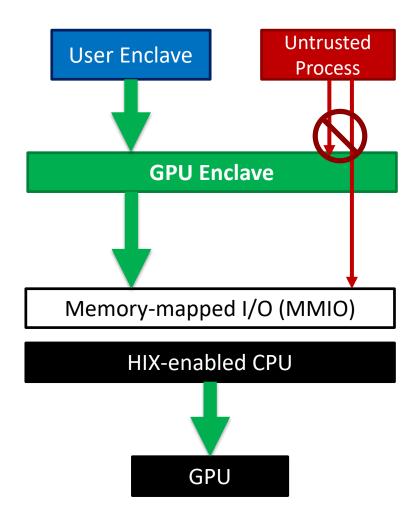
HIX Architecture

- Trusted GPU Device Driver: GPU Enclave
- MMIO Protection
- Inter-Enclave Communication

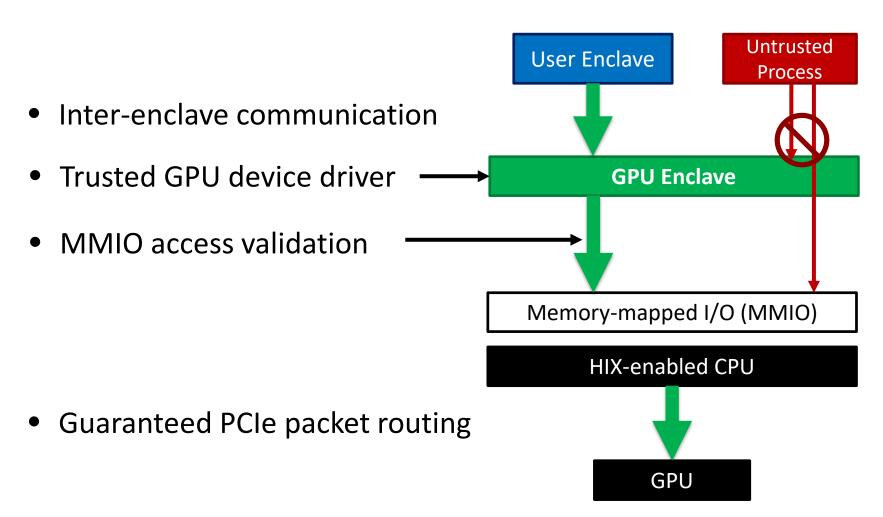
HIX: Architecture Overview



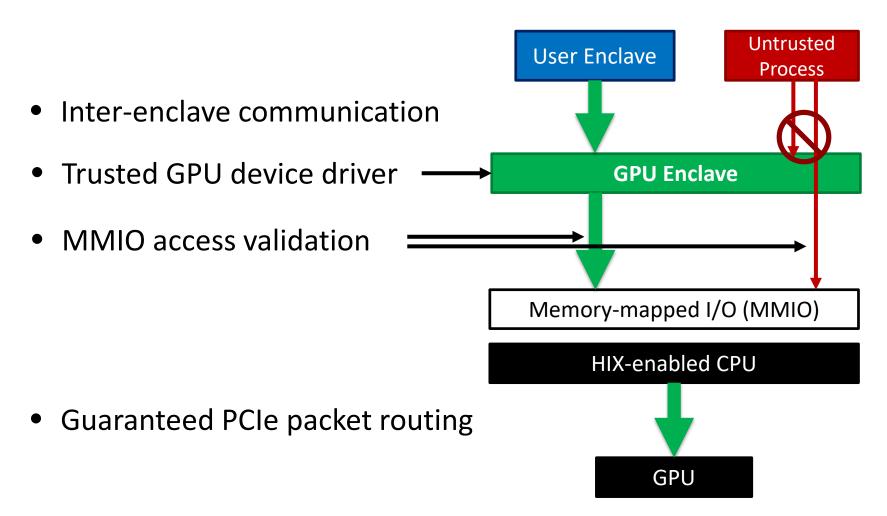
: Three communication paths to be protected



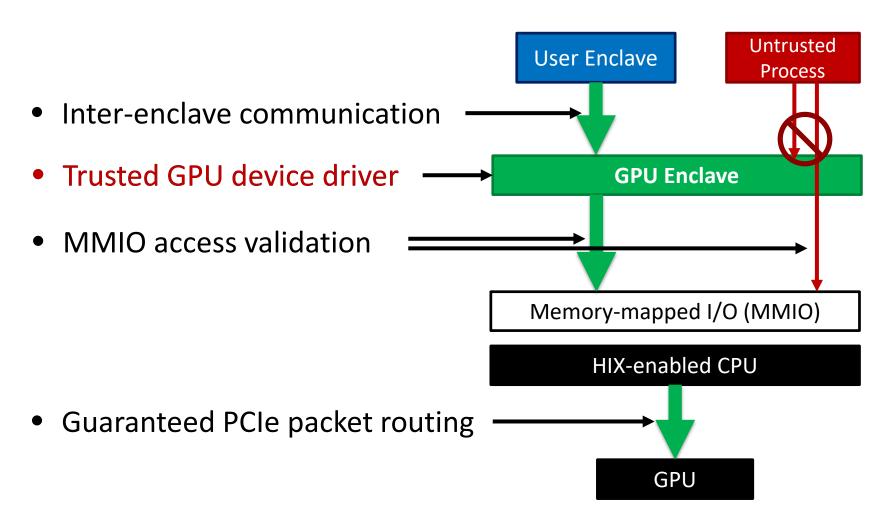




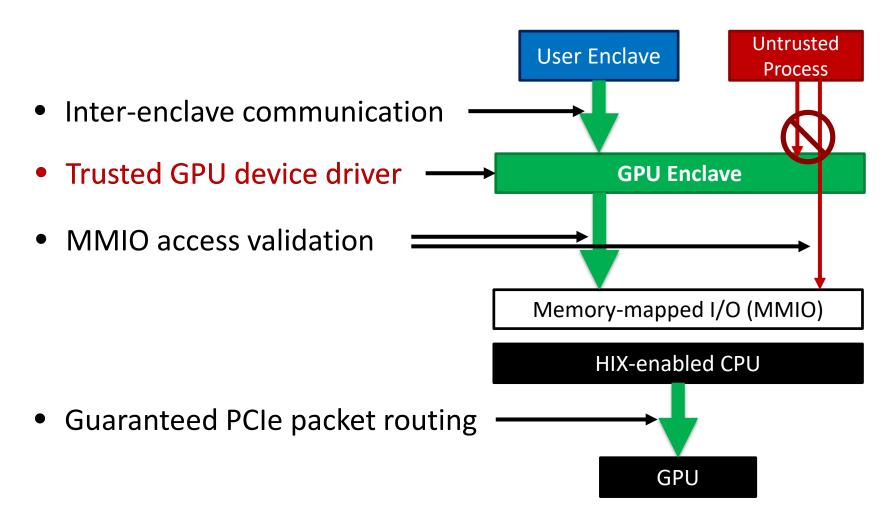




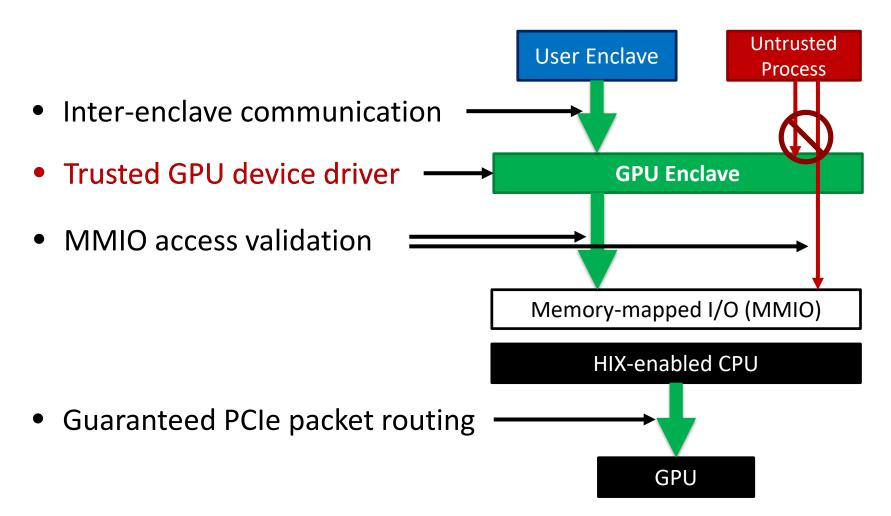
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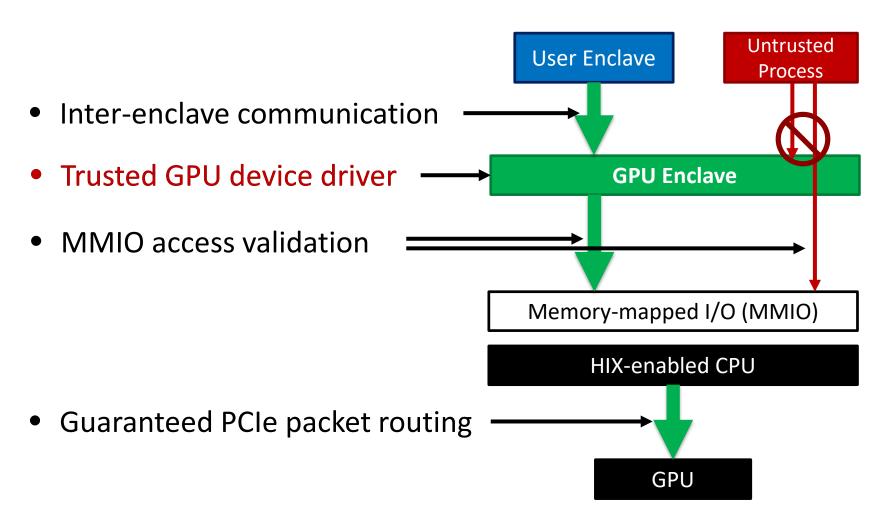
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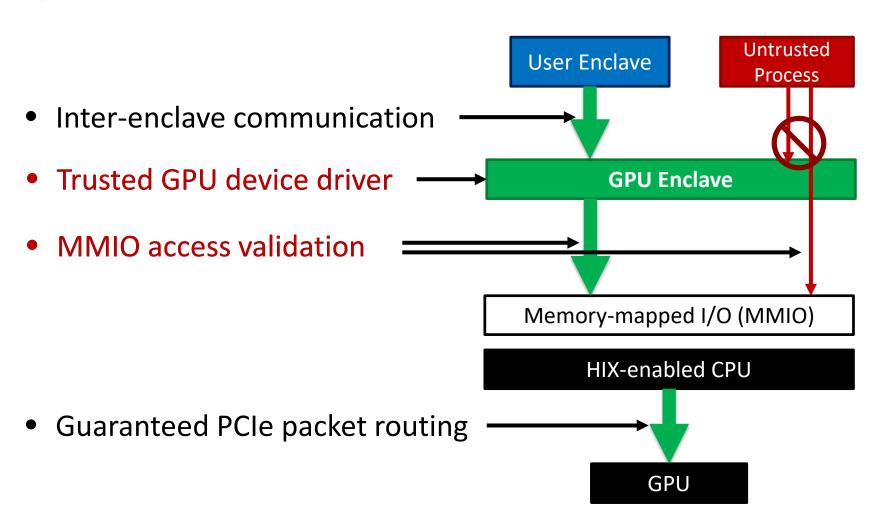
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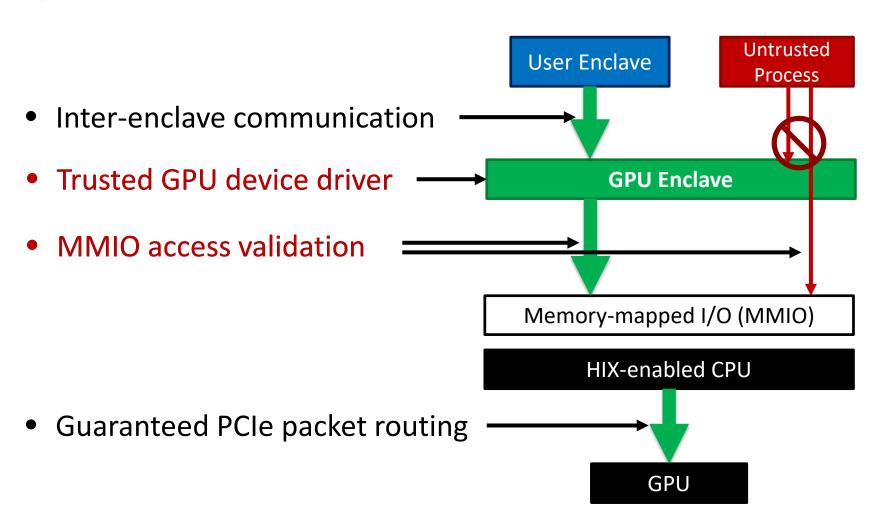




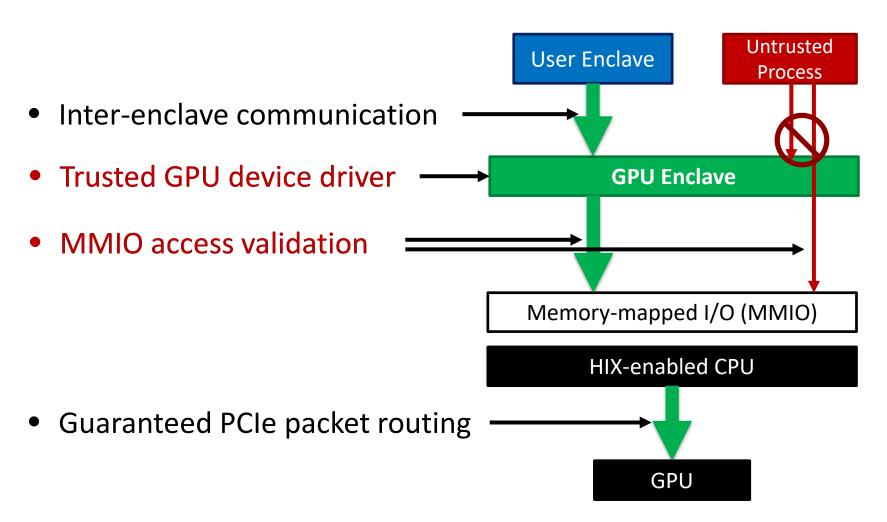




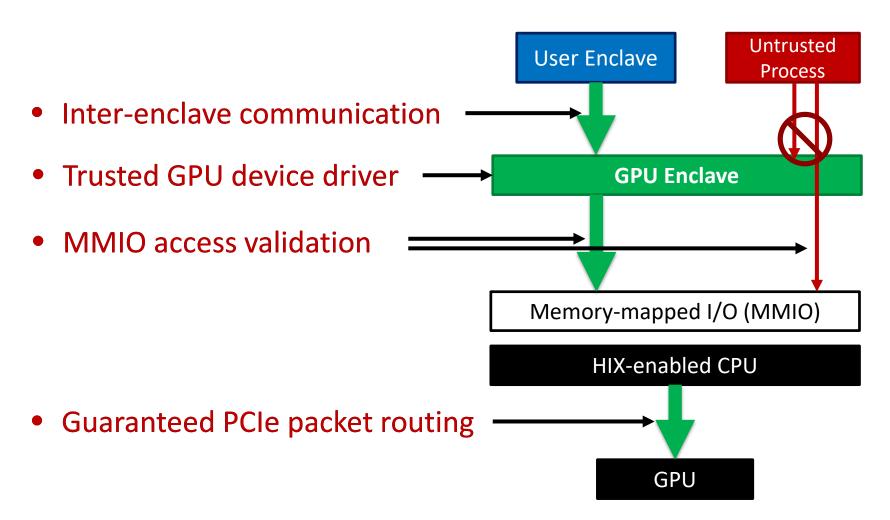




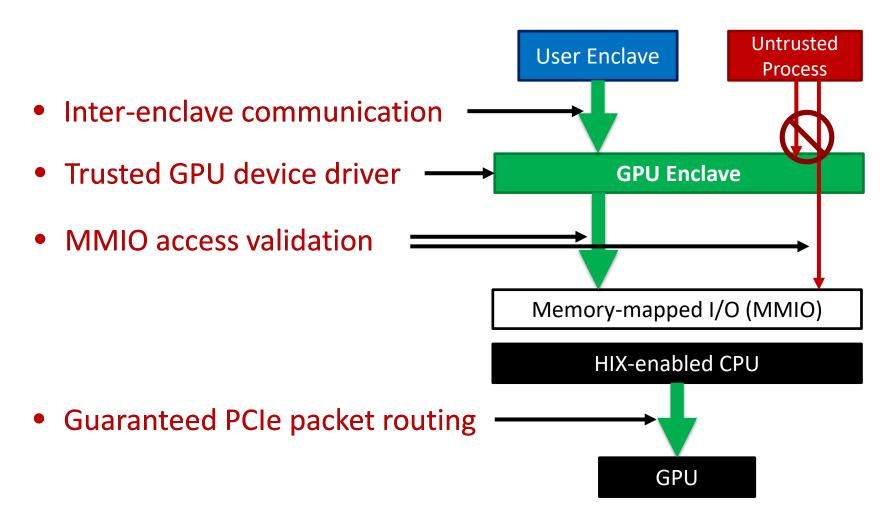




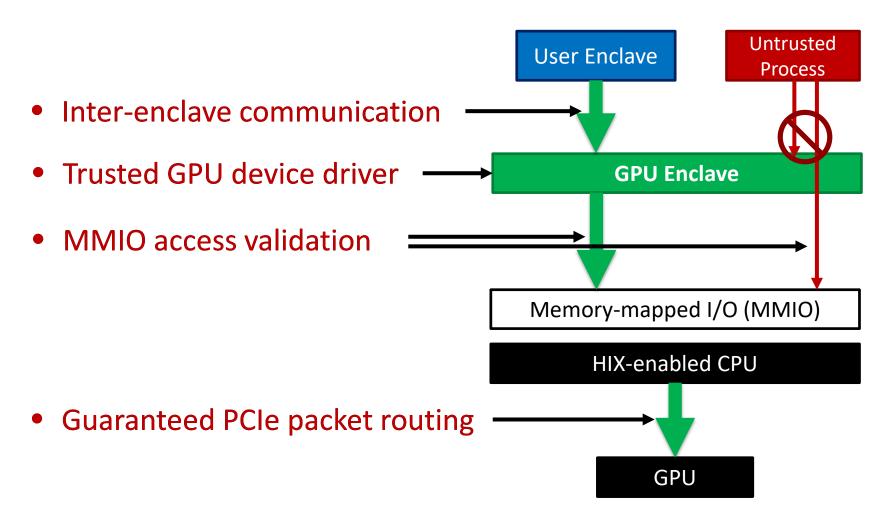




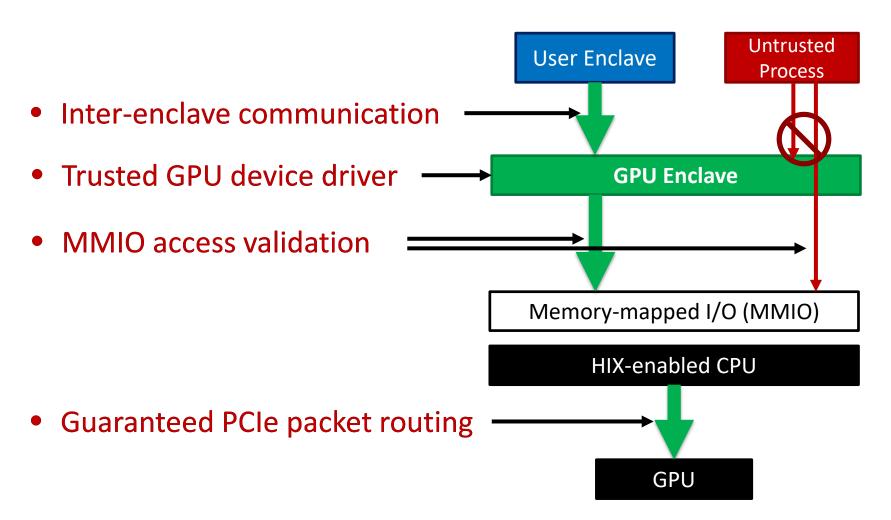






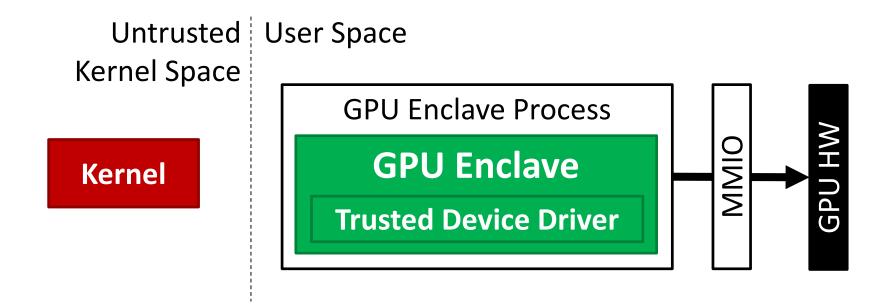






GPU Enclave: Trusted Device Driver

- Move device driver from untrusted kernel space to trusted enclave
- Extended SGX enclave that owns and controls GPU in TEE

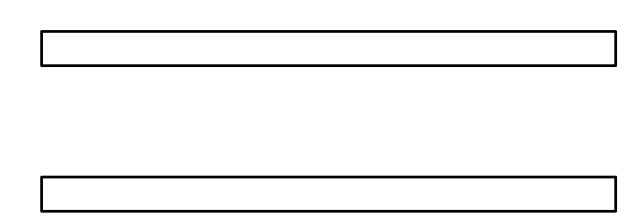


Exclusively access to GPU in the system through MMIO

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Virtual Address Space

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Virtual Address Space	Virtual Address Space	

Physical Address Space

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Virtual Address Space	
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Physical Address Space

DRAM



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Physical Address Space

GPU





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Physical Address Space

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GPU

Main Memory

DRAM

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Physical Address Space MMIO PA Main Memory

GPU DRAM

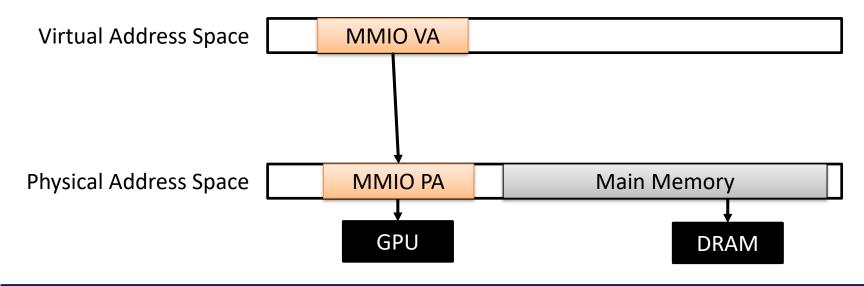
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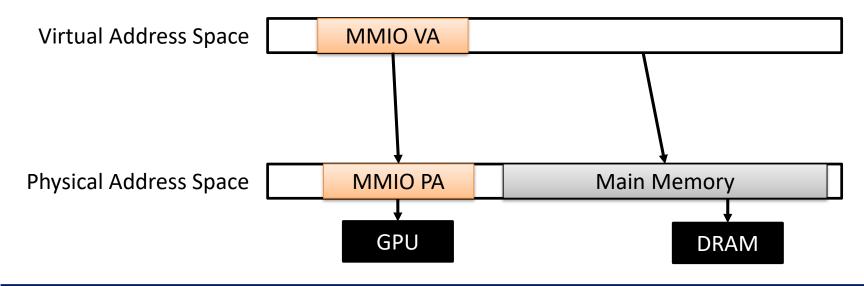
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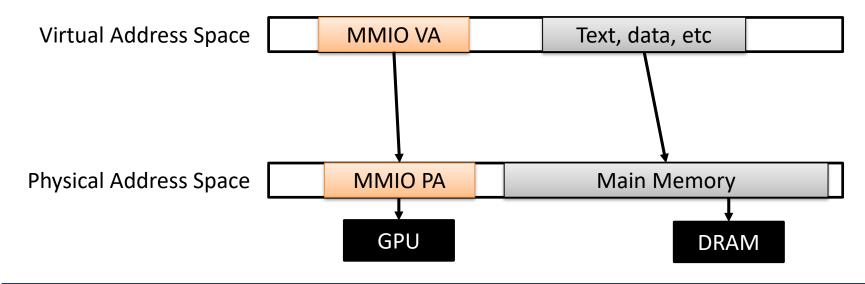
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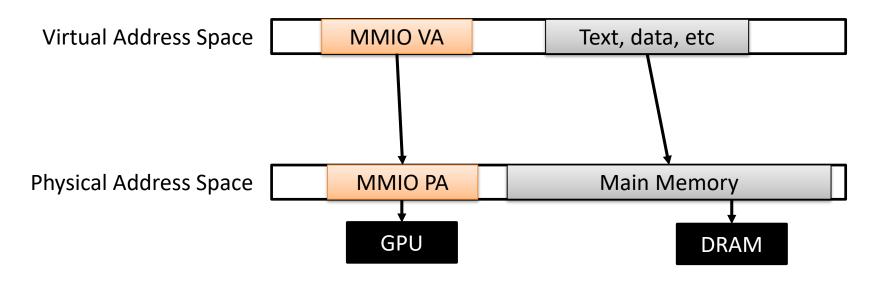


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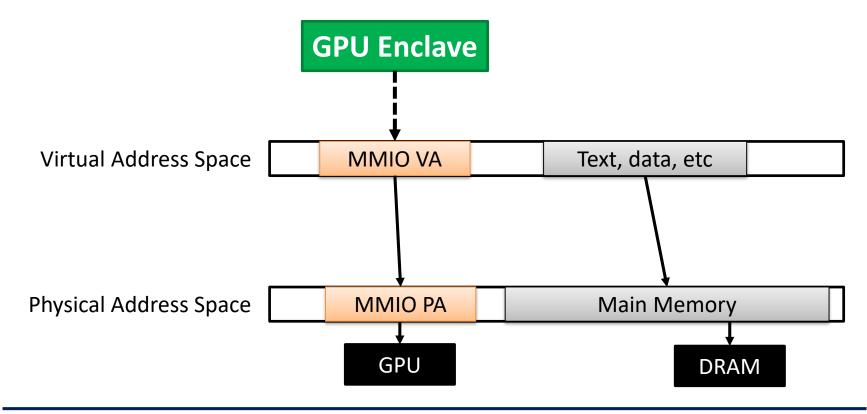


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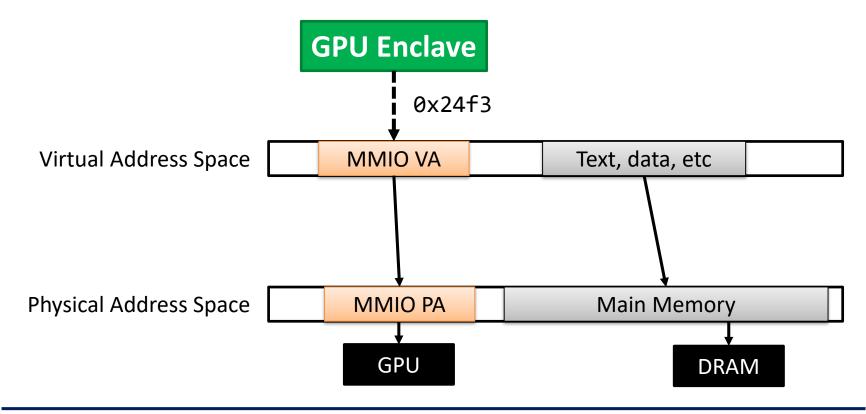
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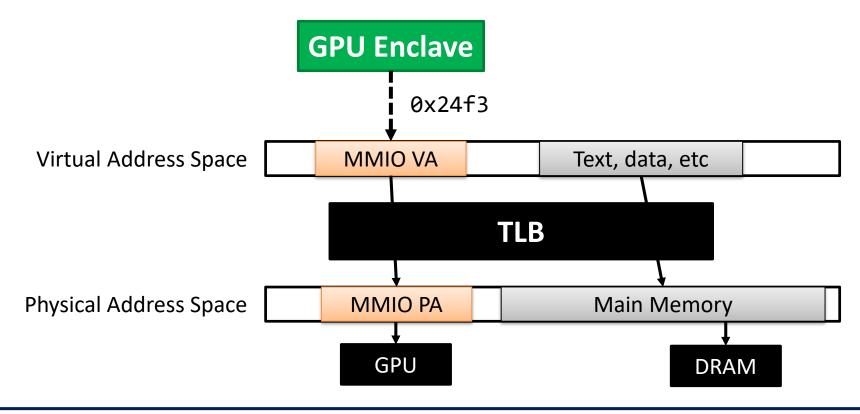
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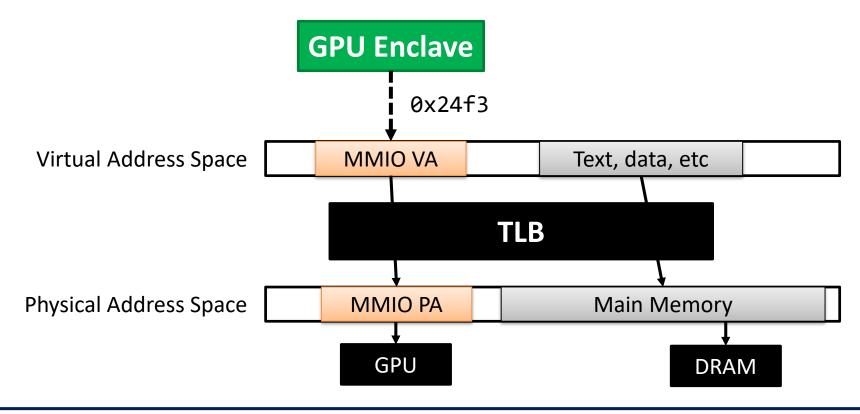
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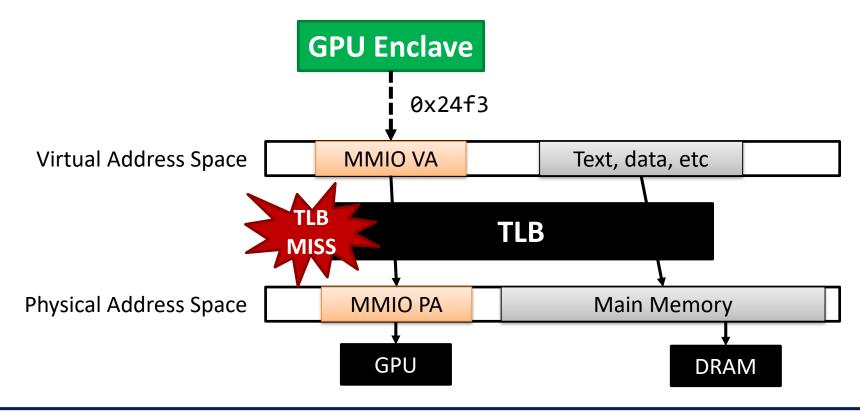
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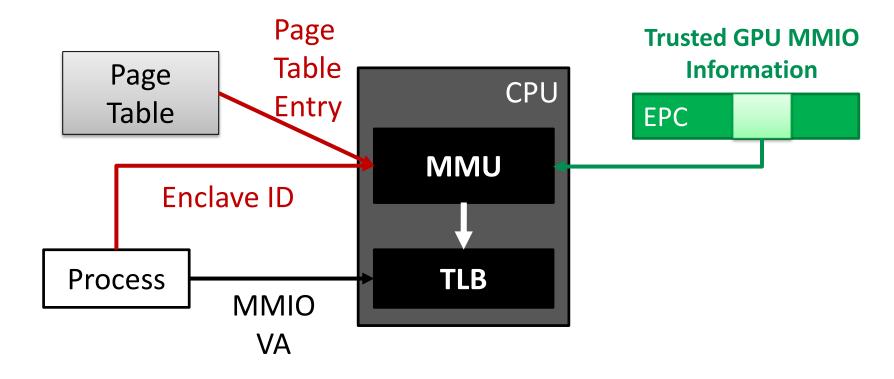
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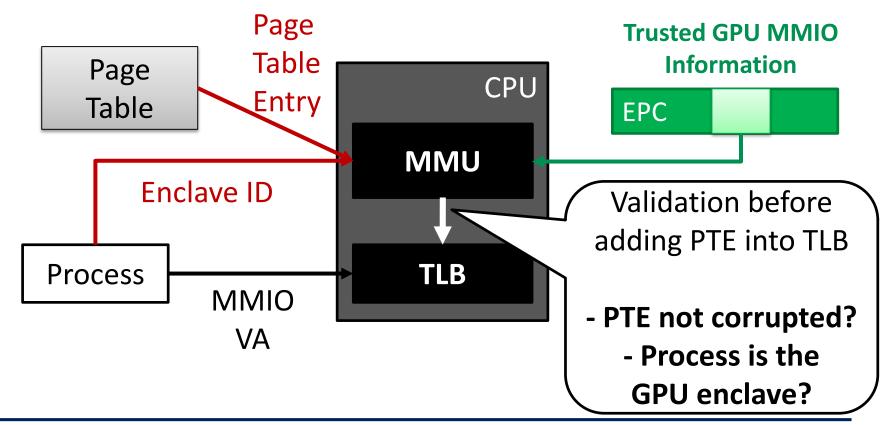


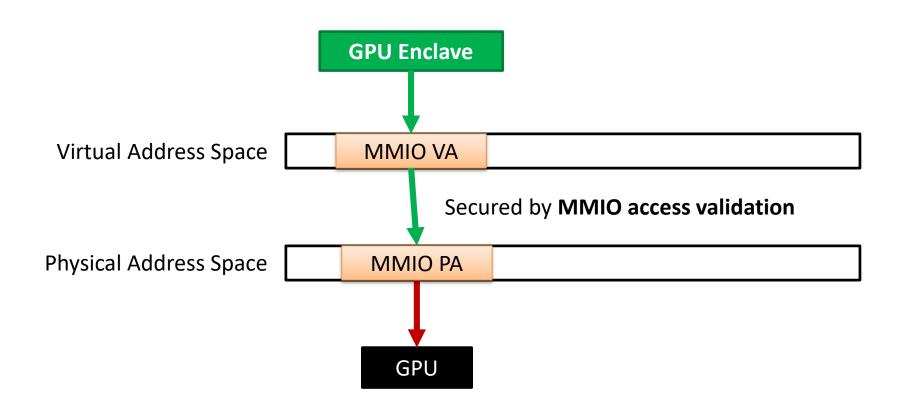
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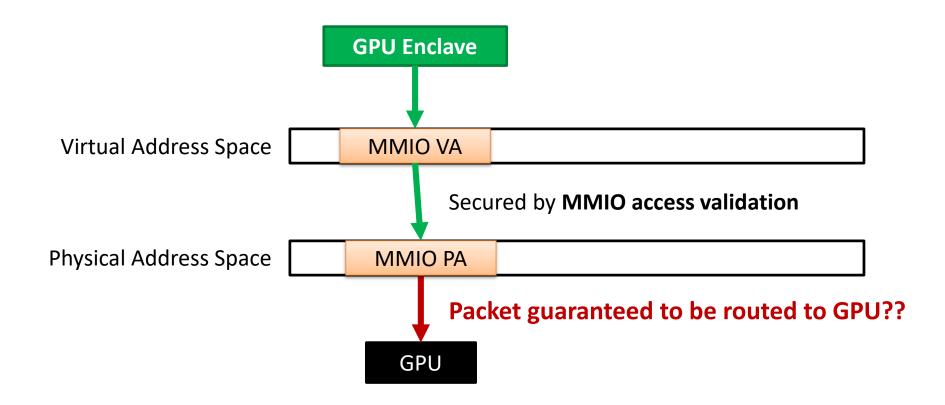


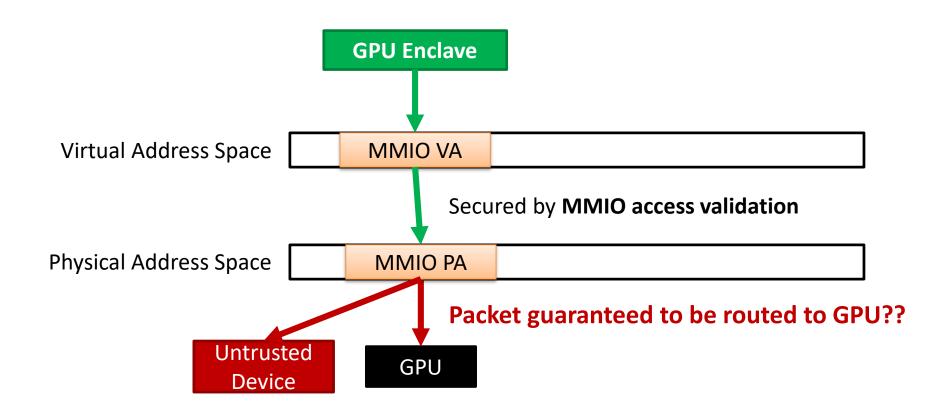
MMIO Access Validation

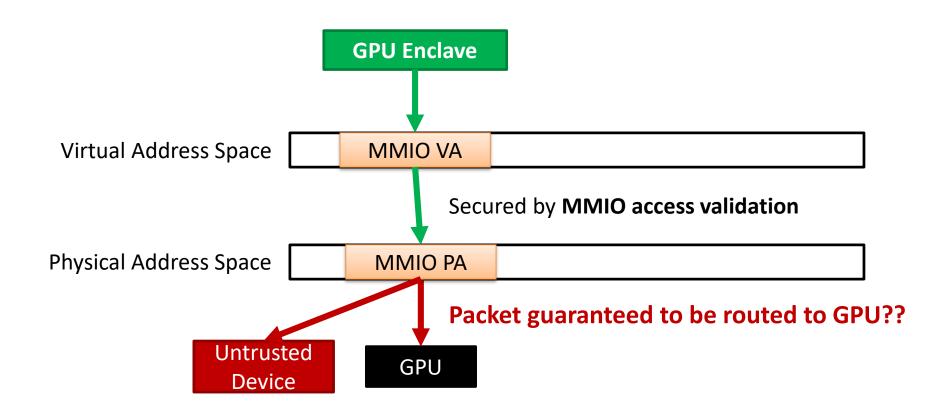
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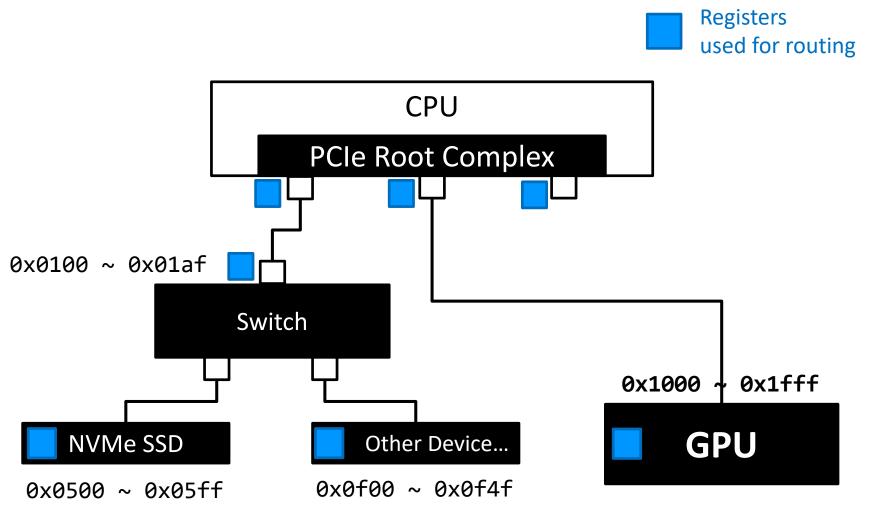


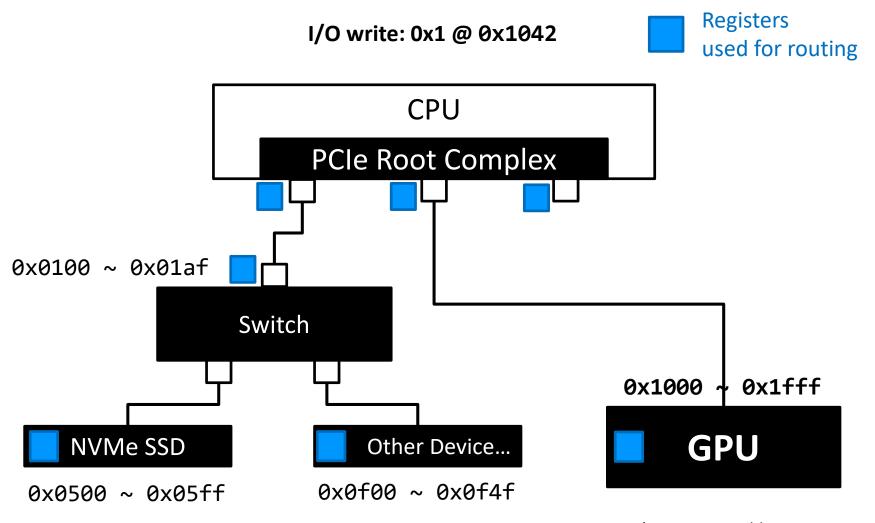


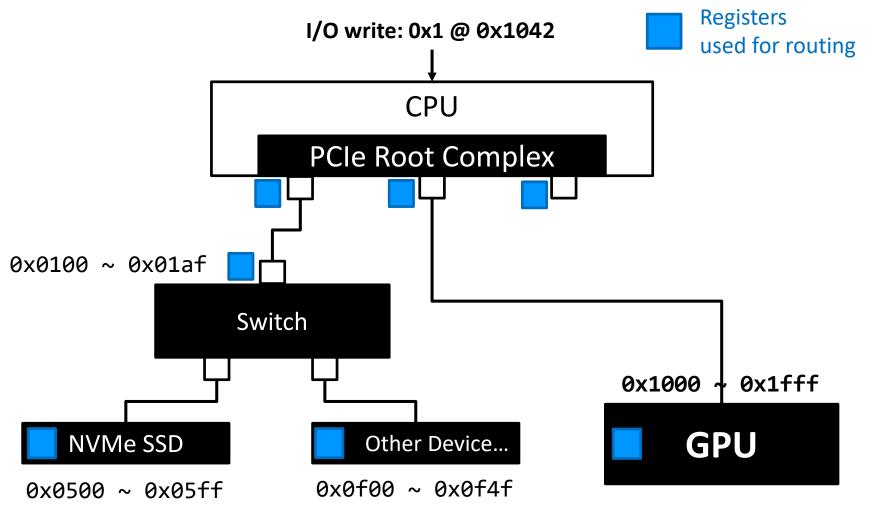


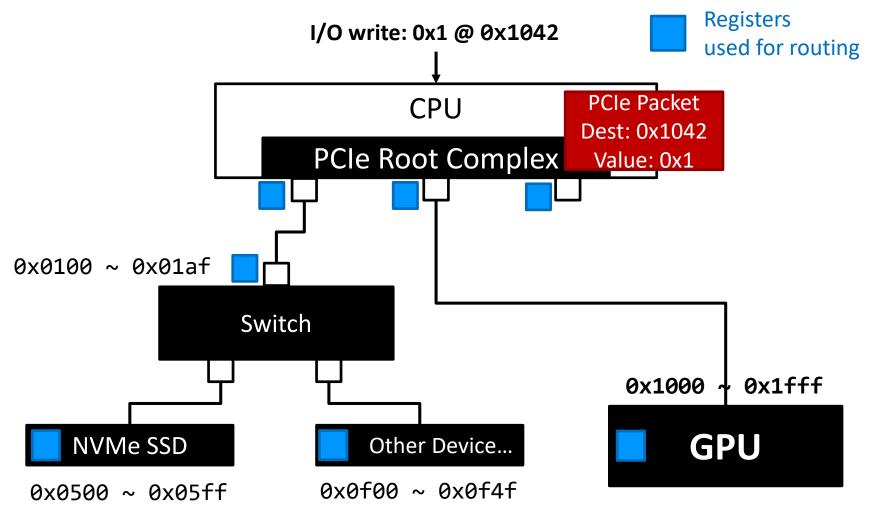


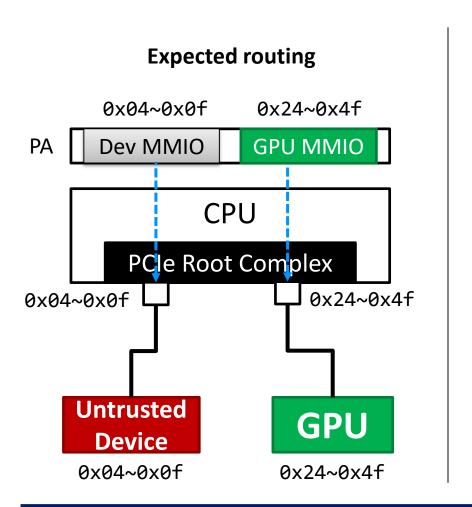


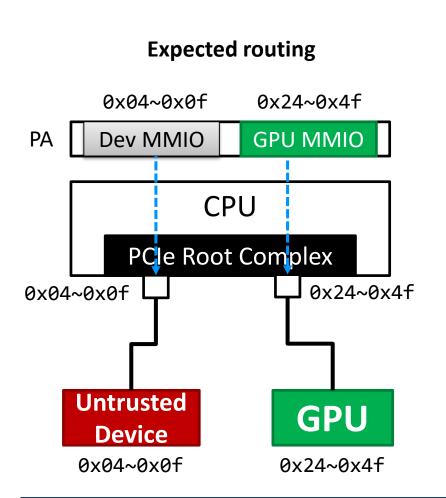


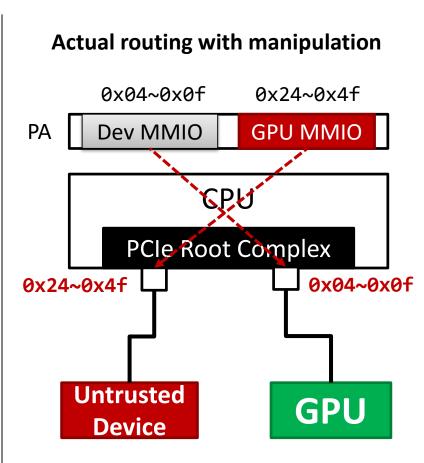


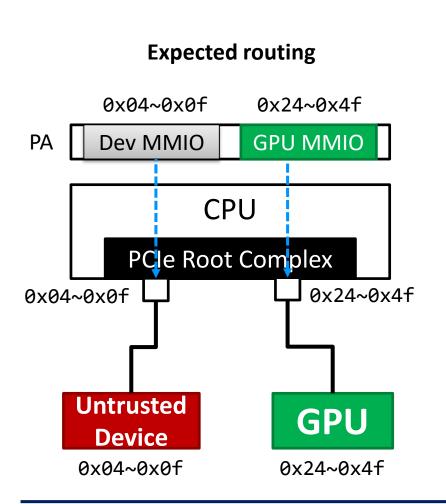


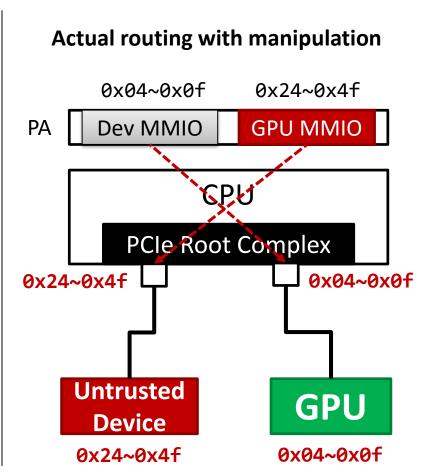


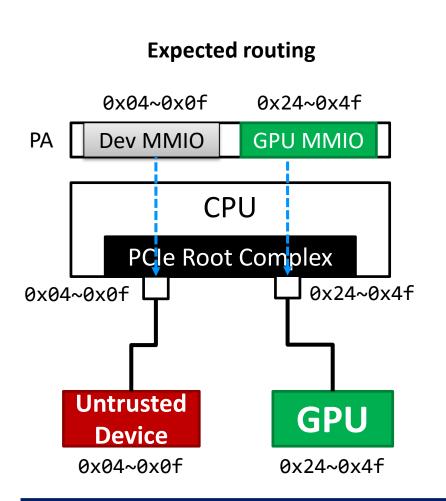


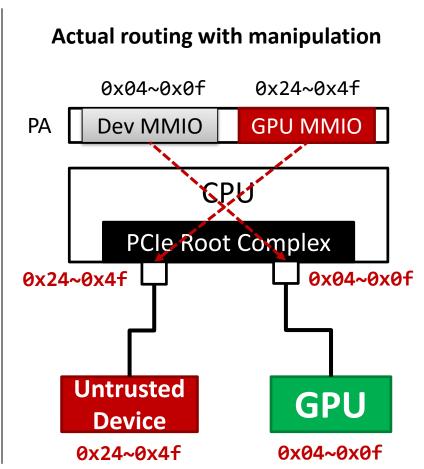




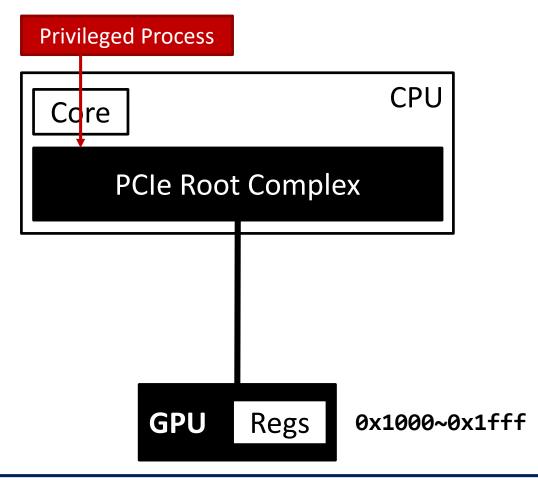




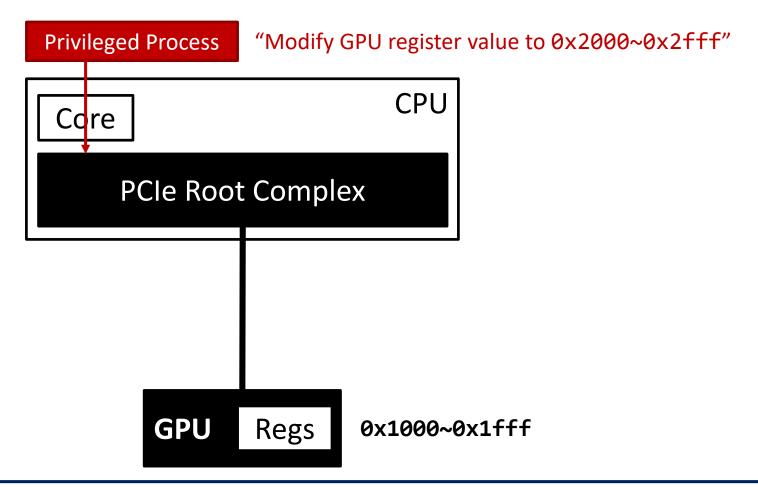




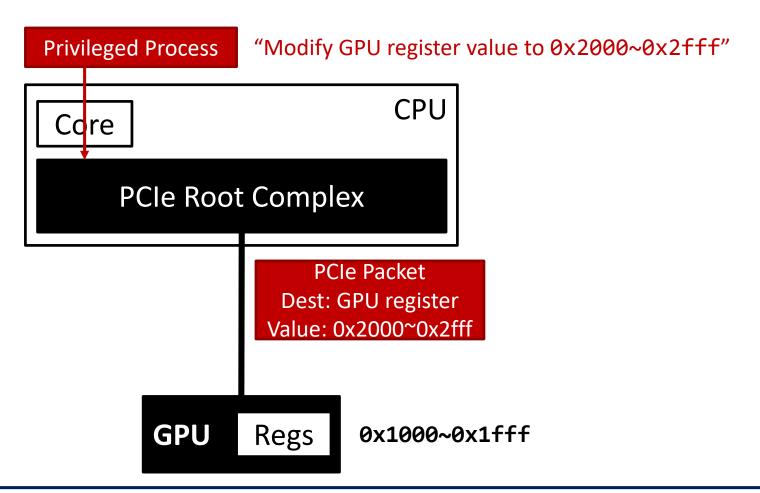
- PCle hardware registers can be manipulated by software
- Solution: freeze MMIO routing information (MMIO lockdown)



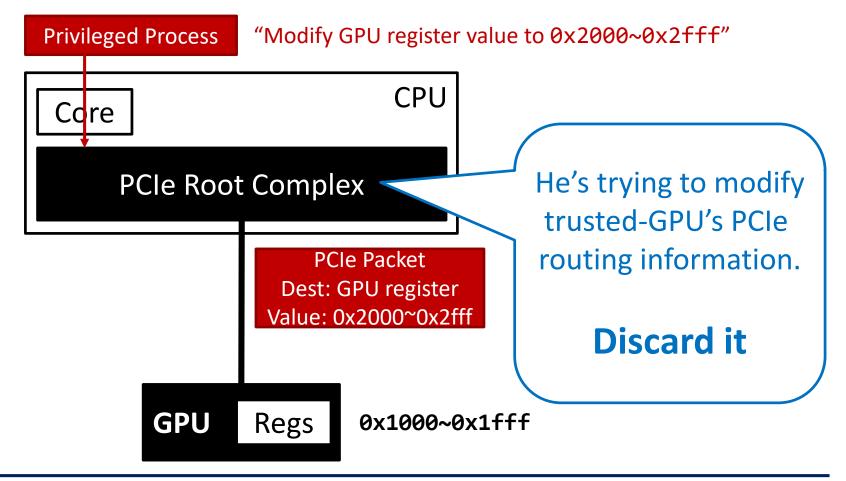
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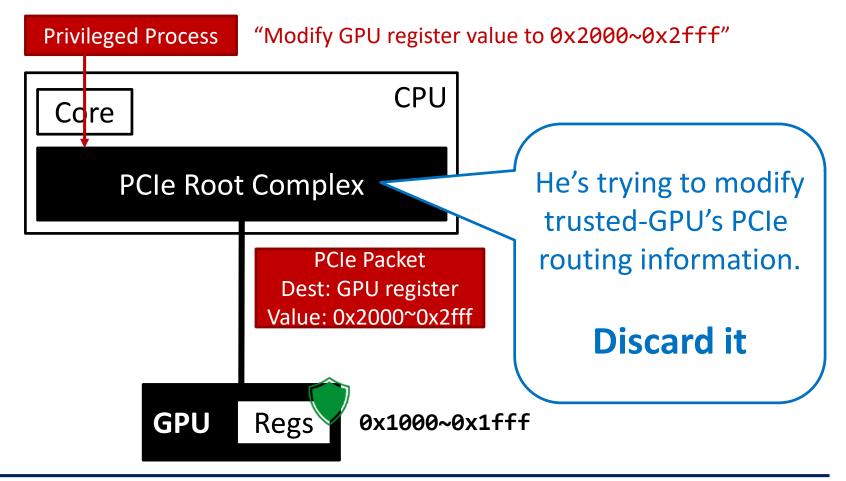
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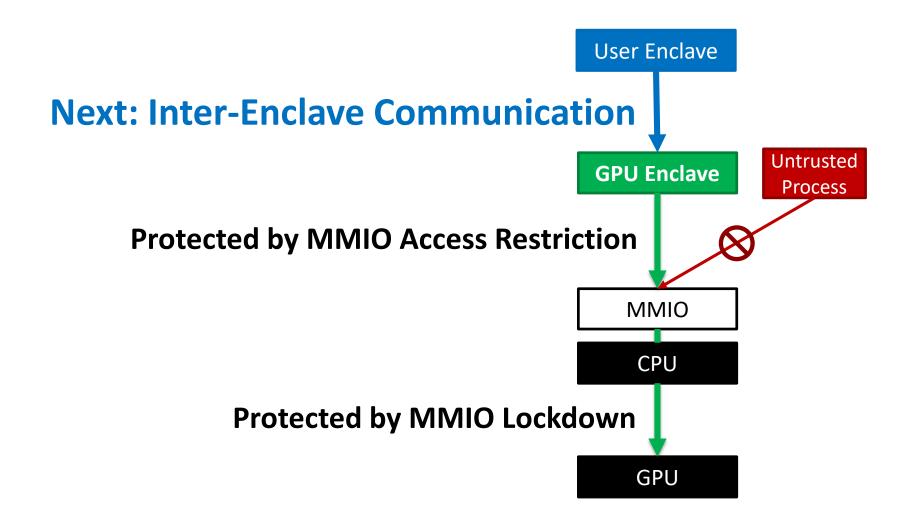
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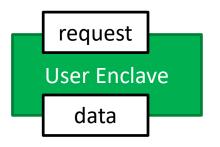
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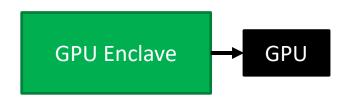


Architecture Review

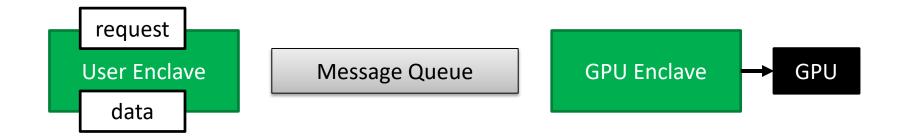


- Inter-process communication: message queue & shared memory
- Confidentiality & integrity provided by authenticated encryption

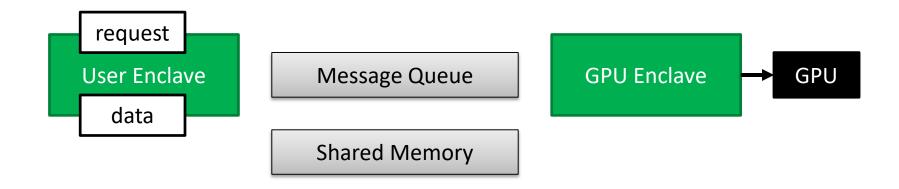




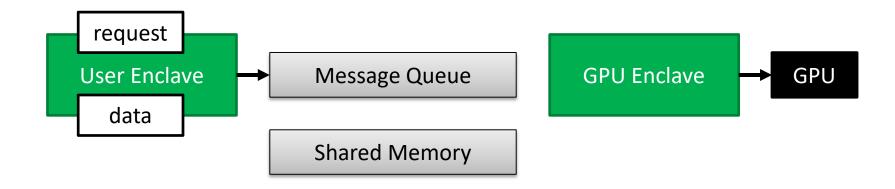
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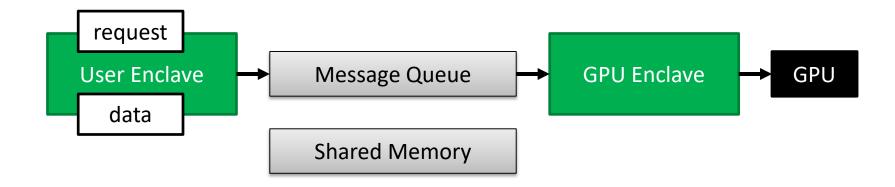
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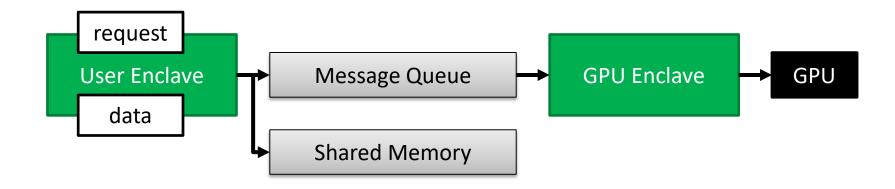
- Inter-process communication: message queue & shared memory
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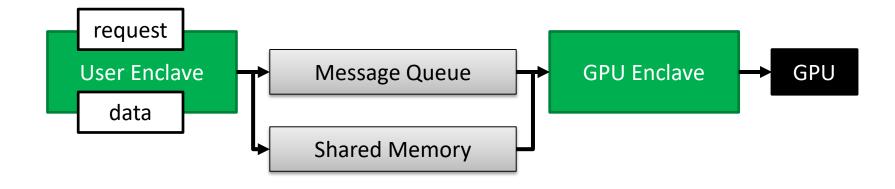
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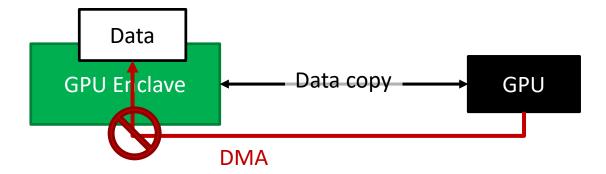
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- Confidentiality & integrity provided by authenticated encryption



Communication Challenge: DMA

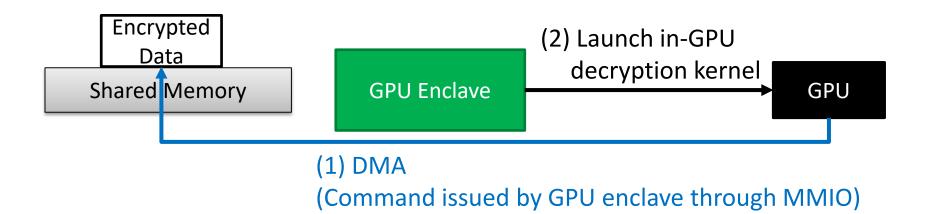
Challenge

- DMA from device to enclaves not allowed by SGX
- Data copy can only be done through (slow) MMIO



Trusted DMA Support

- GPU DMAs encrypted data from shared memory to GPU
- GPU enclave launches in-GPU decryption kernel



Evaluation

Evaluation

- Prototype Implementation
 - Hardware changes are emulated in a KVM/QEMU virtual machine
 - GPU enclave implementation is based on Gdev [Kato, ATC'12]

- Performance analysis: Rodinia GPU microbenchmark
 - Measure overheads due to cryptography, etc.
 - Baseline: unmodified Gdev NVIDIA GPU driver

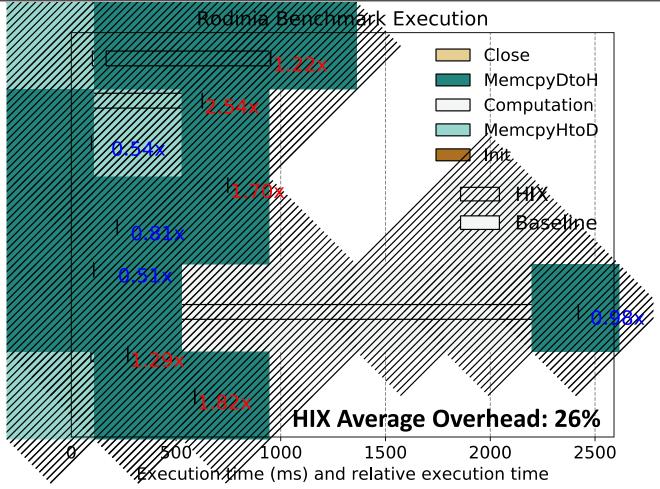
	Baseline	HIX			
Trusted Execution	No	Yes			
Encryption	N/A	AES-OCB [Rogaway '14]			
GPU	NVIDIA Geforce GTX 580*				

^{*} Newer devices are not supported by Gdev

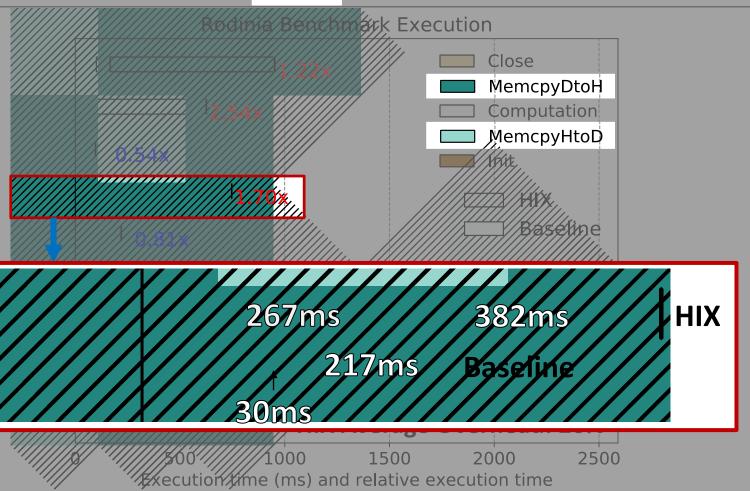


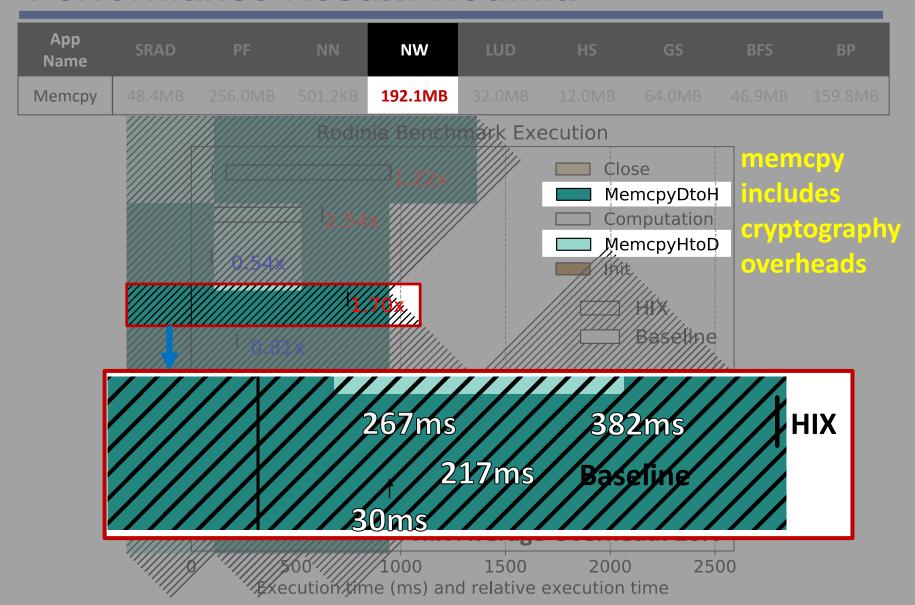


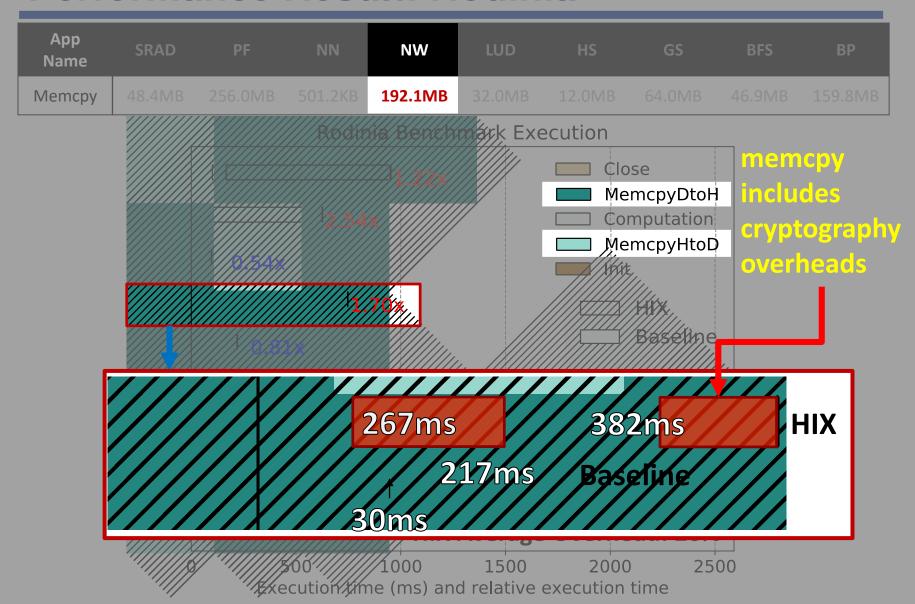
App Name	SRAD	PF	NN	NW	LUD	HS	GS	BFS	ВР
Memcpy	48.4MB	256.0MB	501.2KB	192.1MB	32.0MB	12.0MB	64.0MB	46.9MB	159.8MB

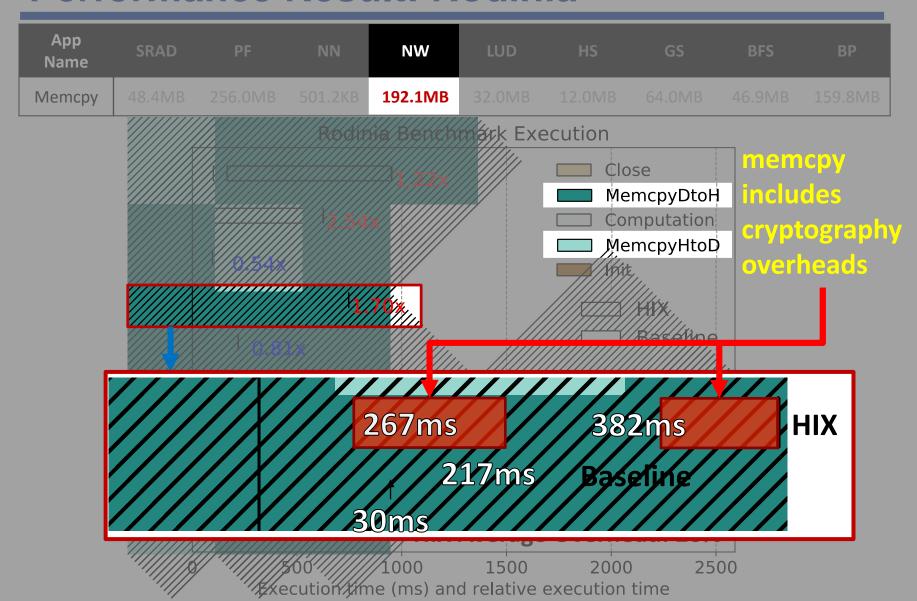


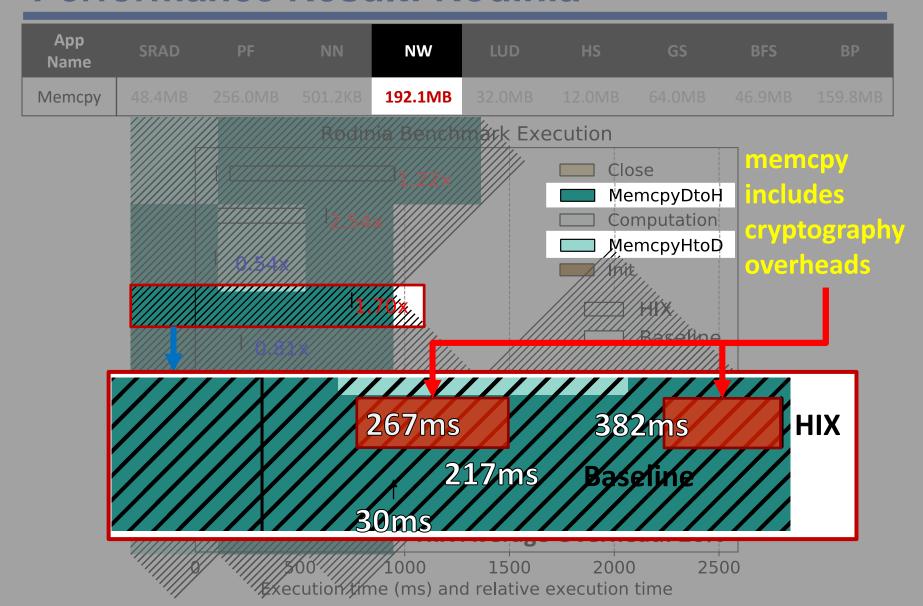
App Name	SRAD	PF	NN	NW	LUD	HS	GS	BFS	ВР
Memcpy	48.4MB			192.1MB					159.8MB

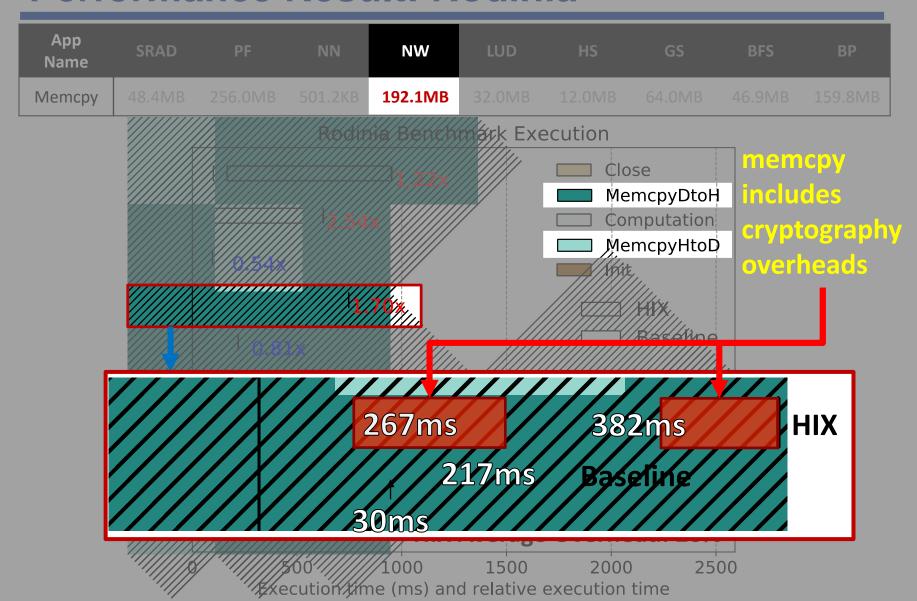




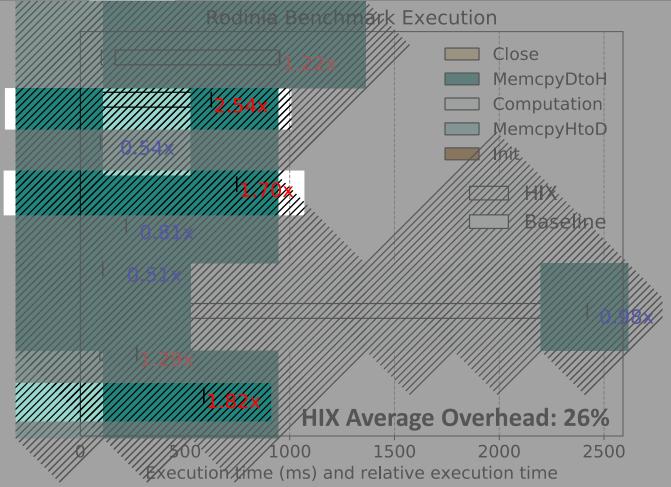




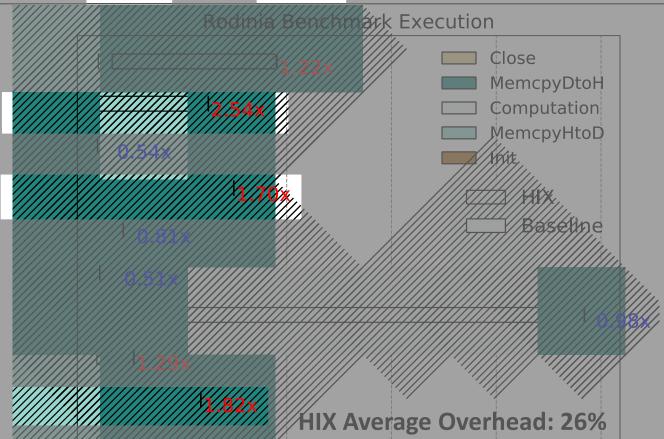




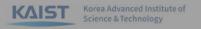
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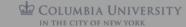


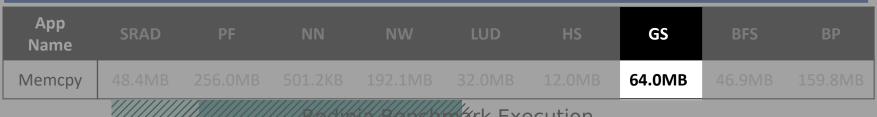
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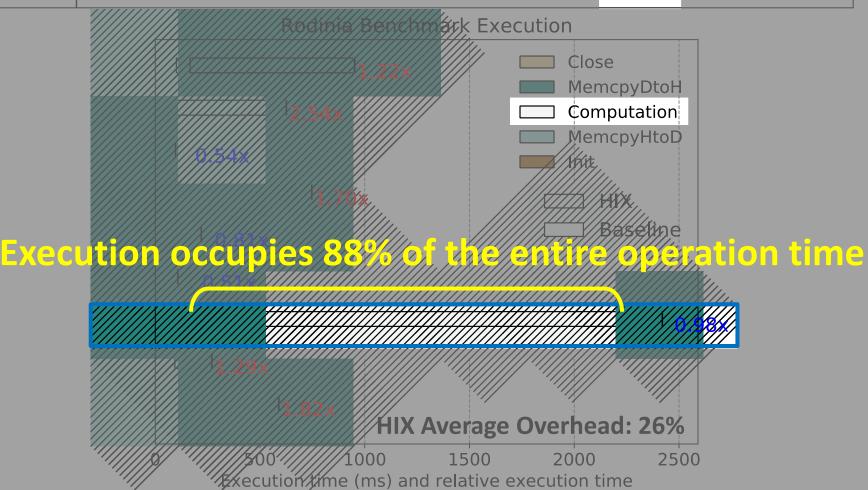


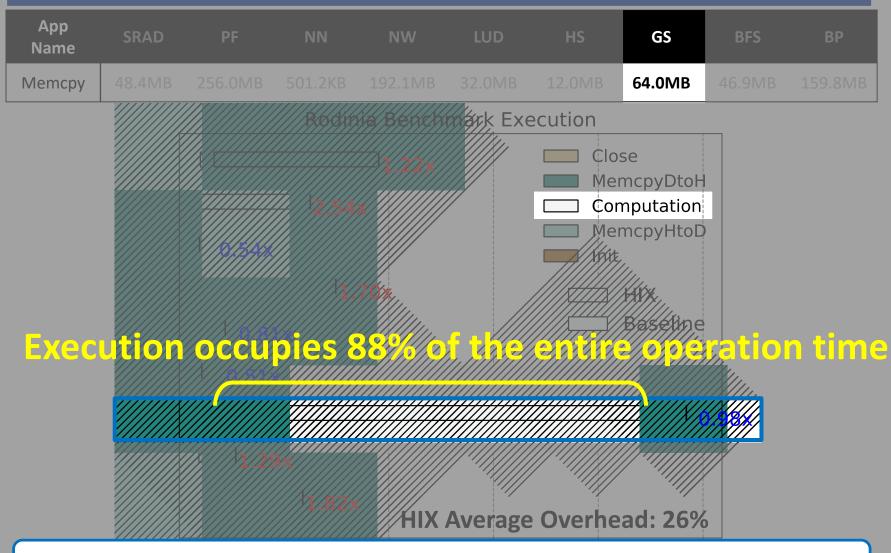
Large Amount of Data → **High Cryptography Overheads**





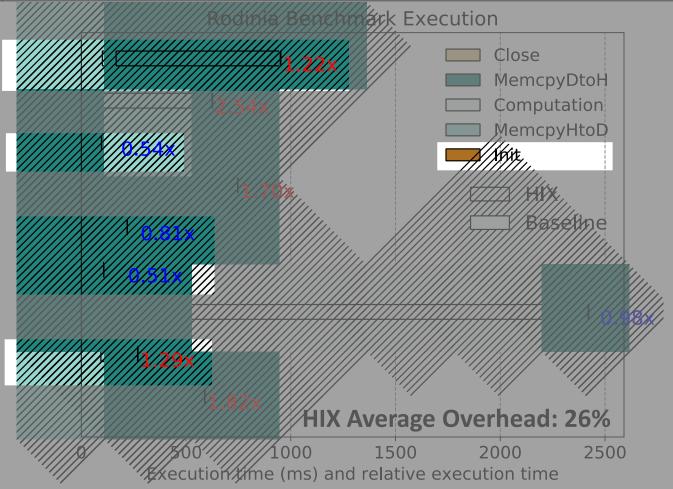




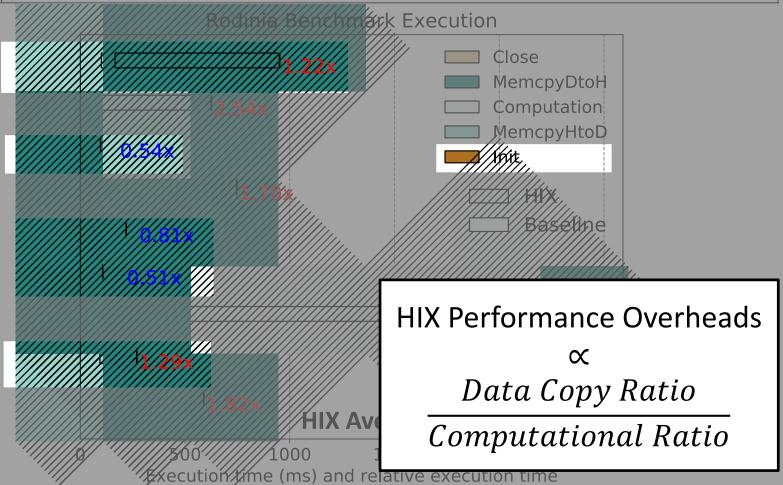


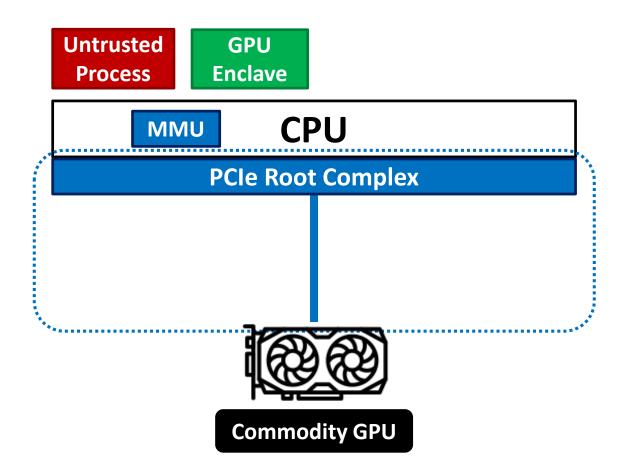
High Computational Ratio → Cryptography Overhead Ratio Reduced

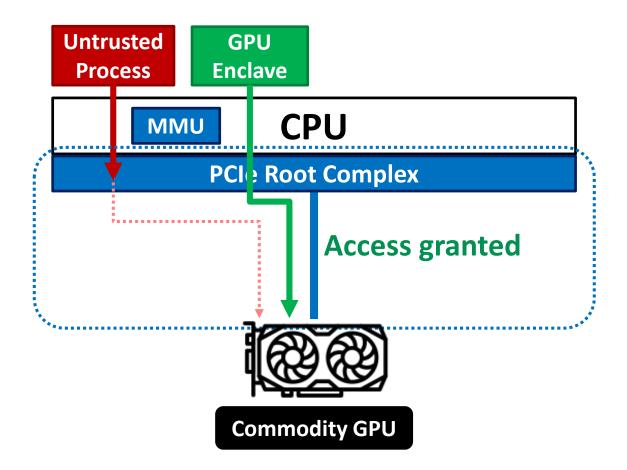
App Name	SRAD	PF	NN	NW	LUD	HS	GS	BFS	ВР
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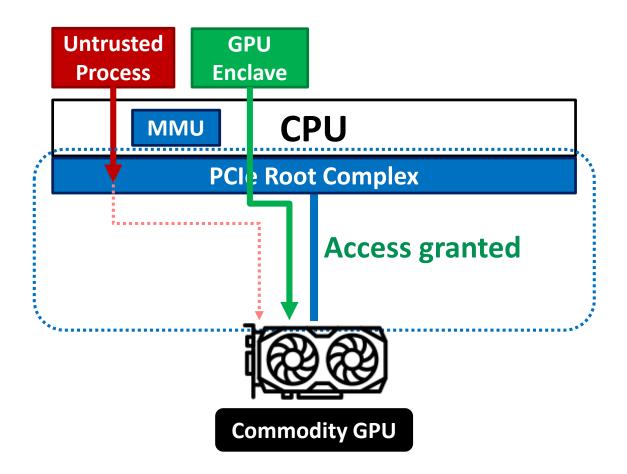


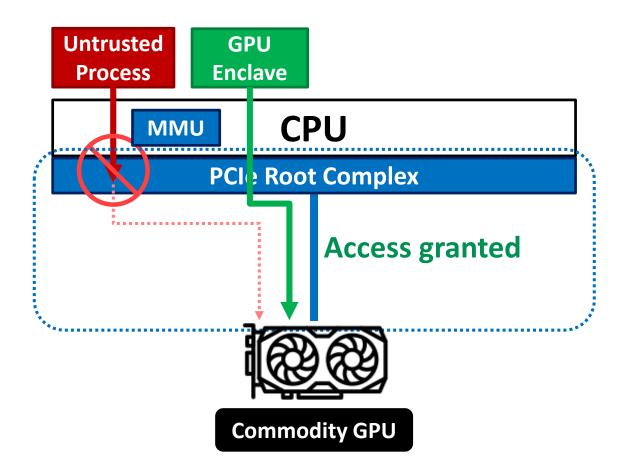
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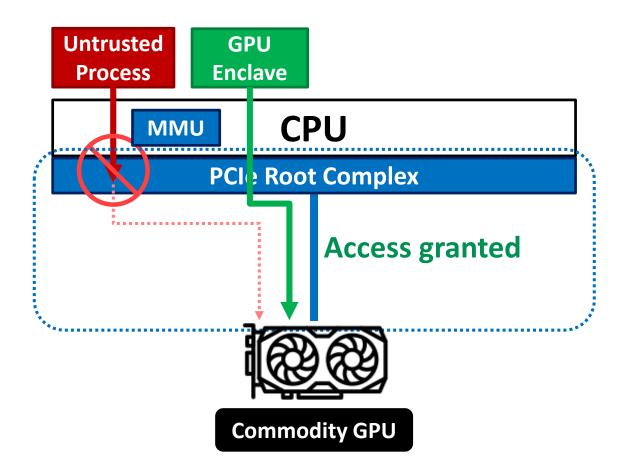


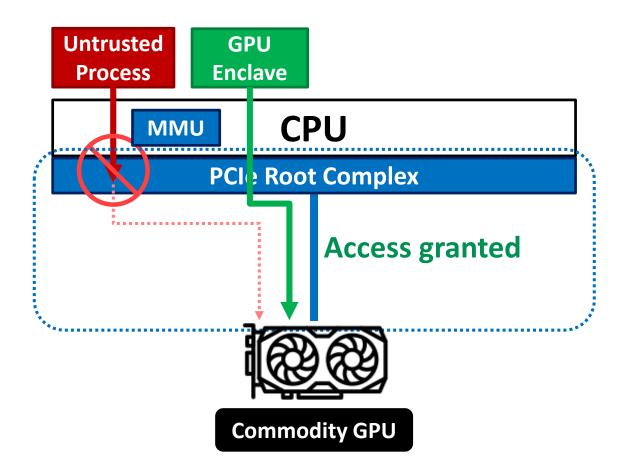


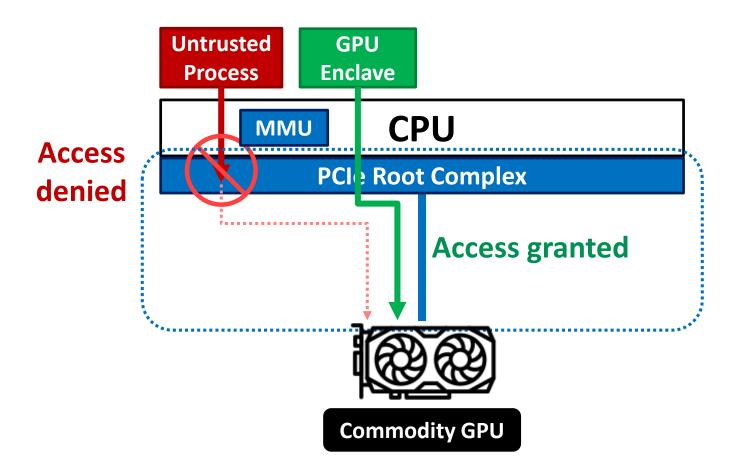






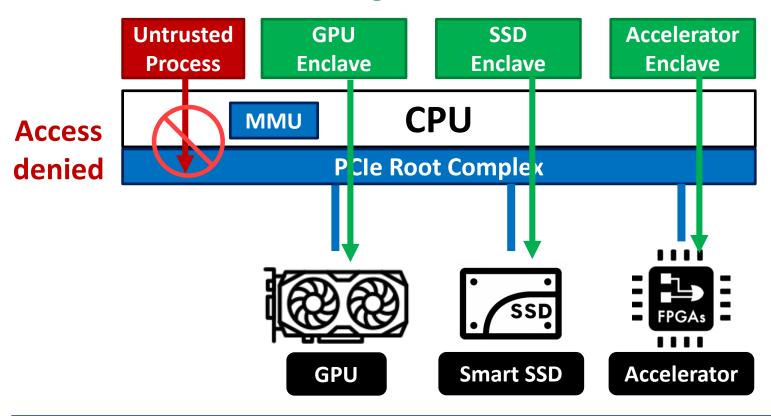






HIX: Provide trusted execution environment to commodity GPUs

Access granted to their own devices



Expandable Device Protection

Heterogeneous Isolated Execution for Commodity GPUs

Thank you for Listening!

Q&A



