# Unified Memory Protection with Multi-granular MAC and Integrity Tree for Heterogeneous Processors

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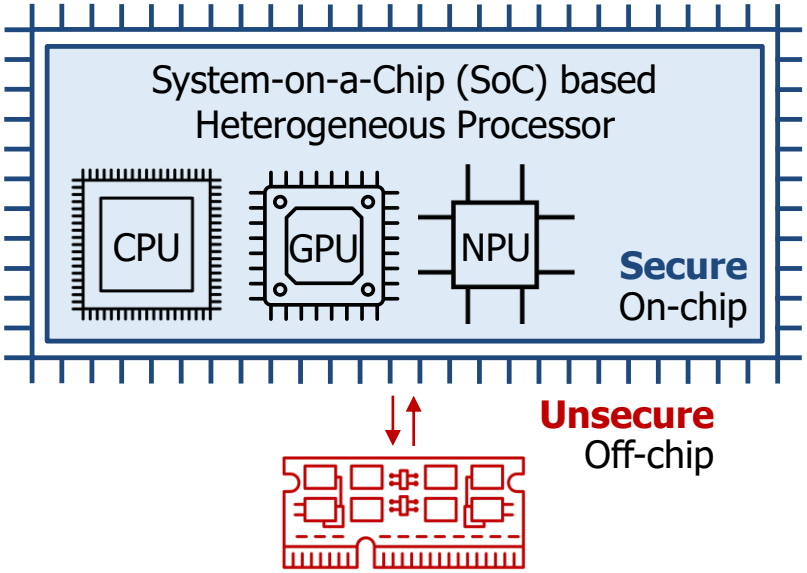
Jinwon Pyo[1], Jaehyuk Huh[1]

KAIST[1], Georgia Tech[2]



# Secure Heterogeneous Processor

- Heterogeneous processor: SoC with CPU, GPU, NPU



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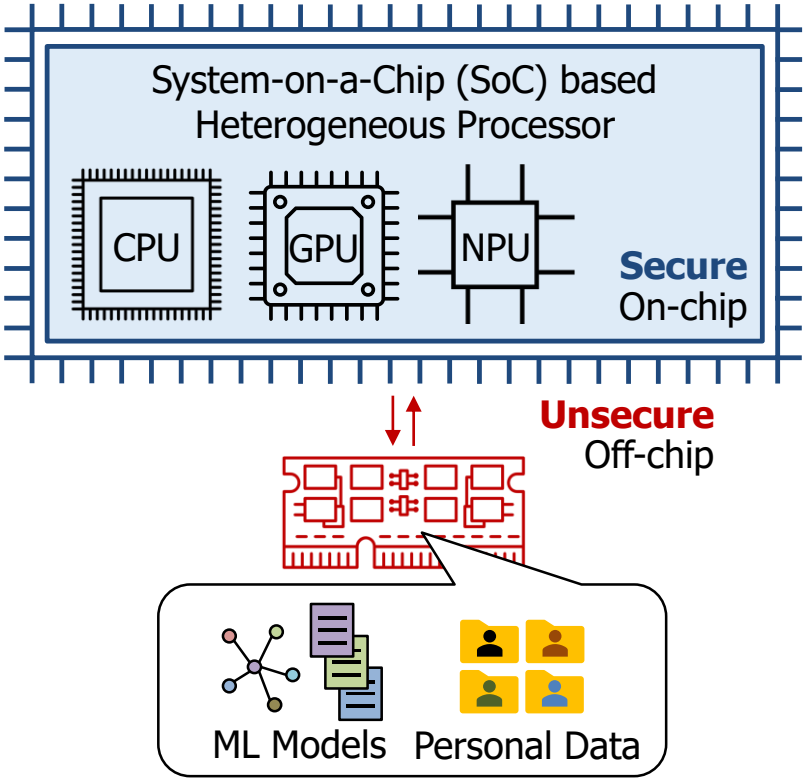


[1] Lest We Remember: Cold-Boot Attacks on Encryption Keys (USENIX Security 2008)
[2] RAMBleed: Reading Bits in Memory Without Accessing Them (S&P 2020)
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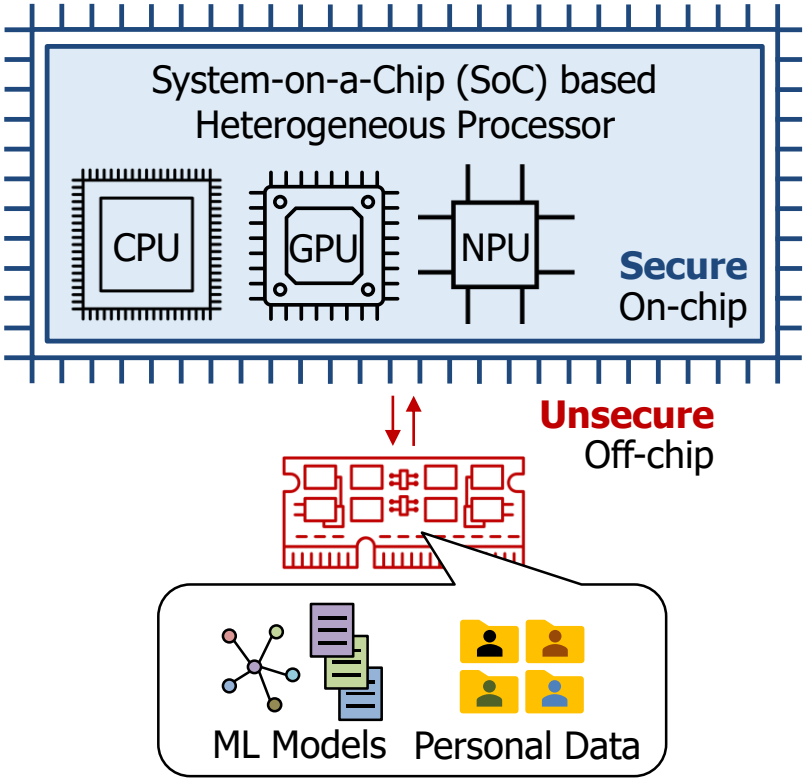
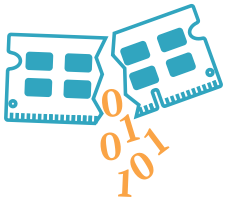
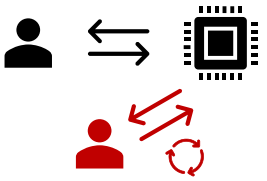



Cold Boot Attack [1]




Rowhammer Attack [2]

DMA Attack [3]



Replay Attack [4]

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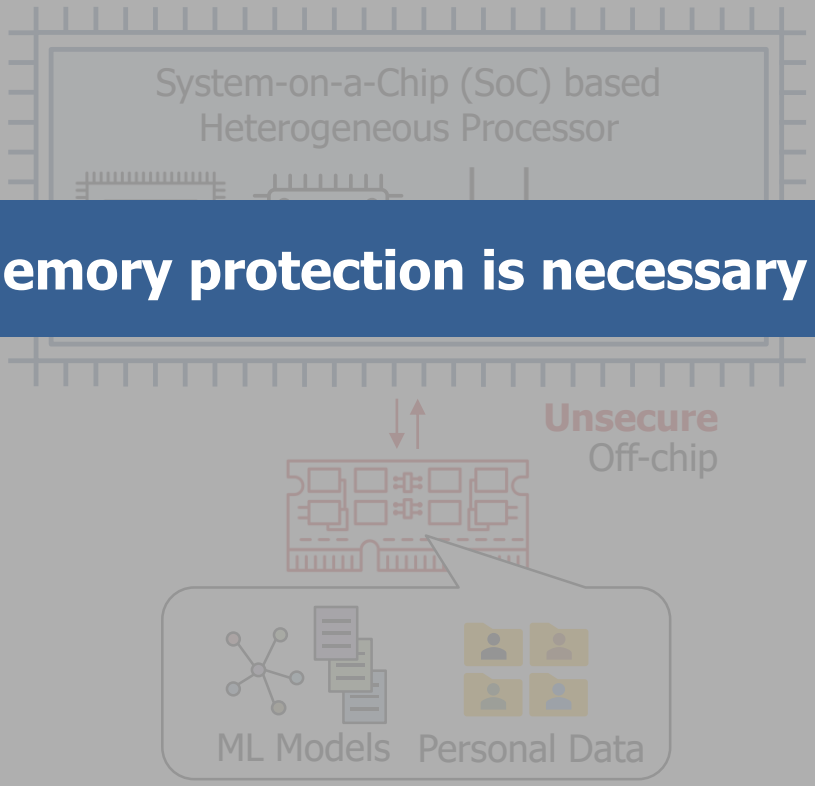


**Memory protection is necessary for heterogeneous processors**


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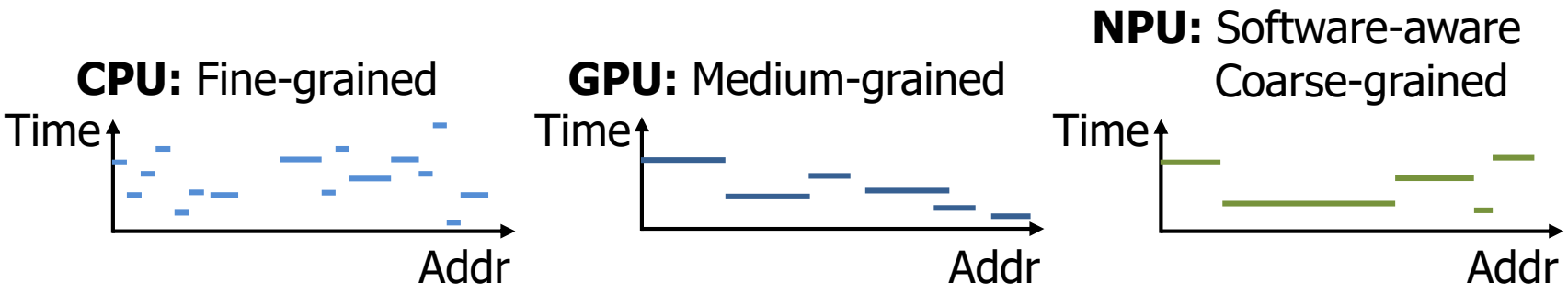

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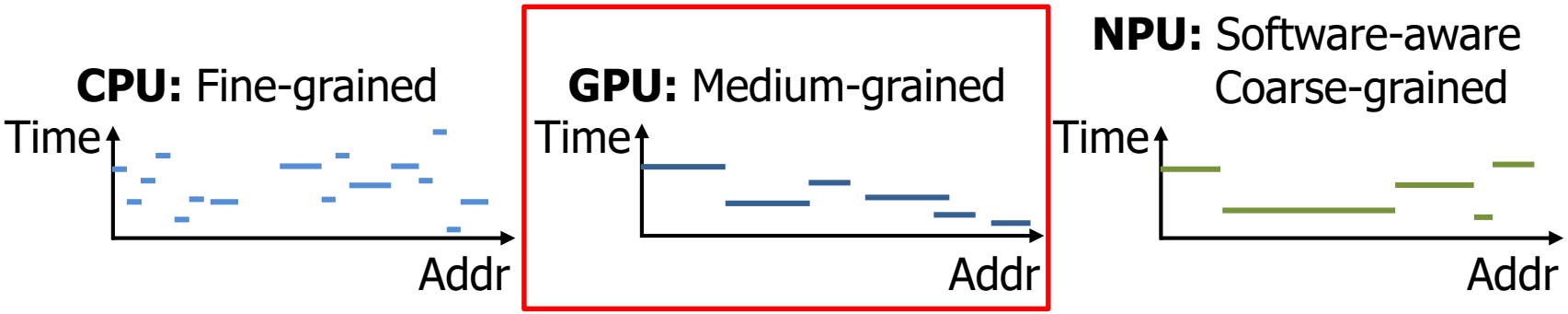


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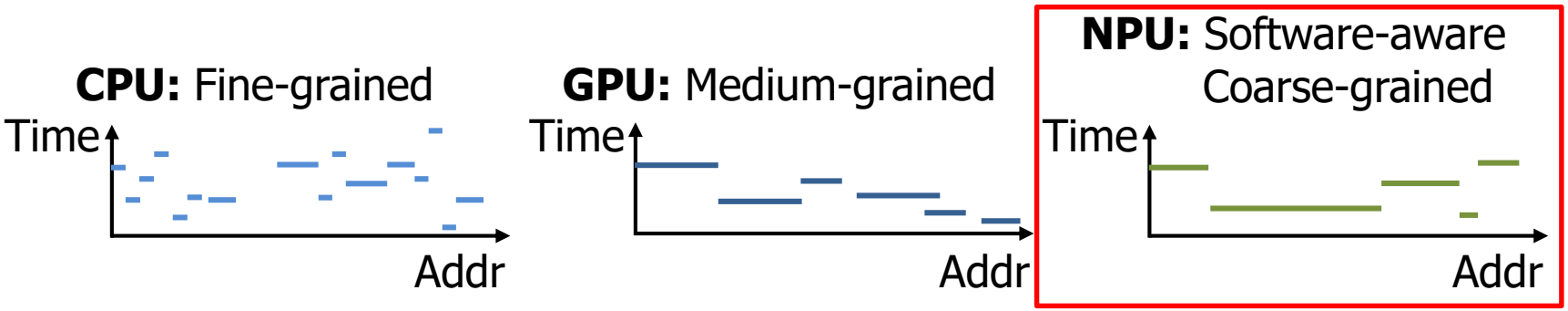


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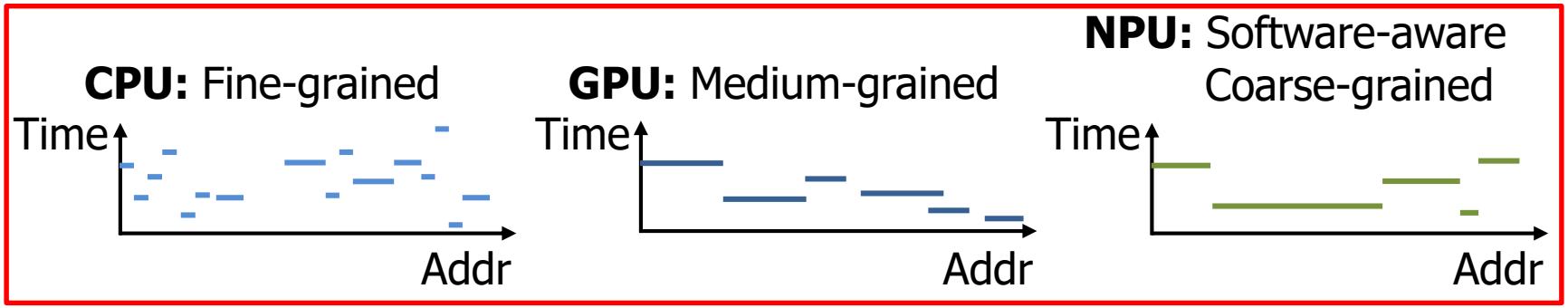


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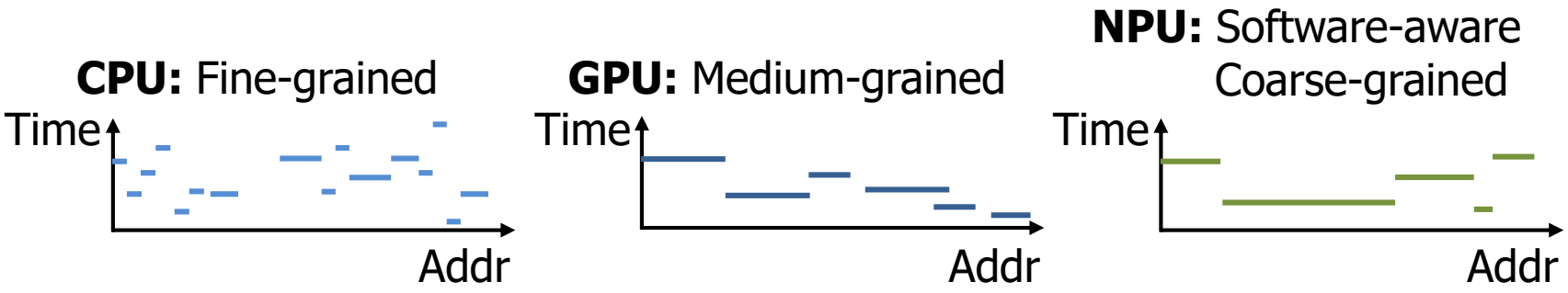


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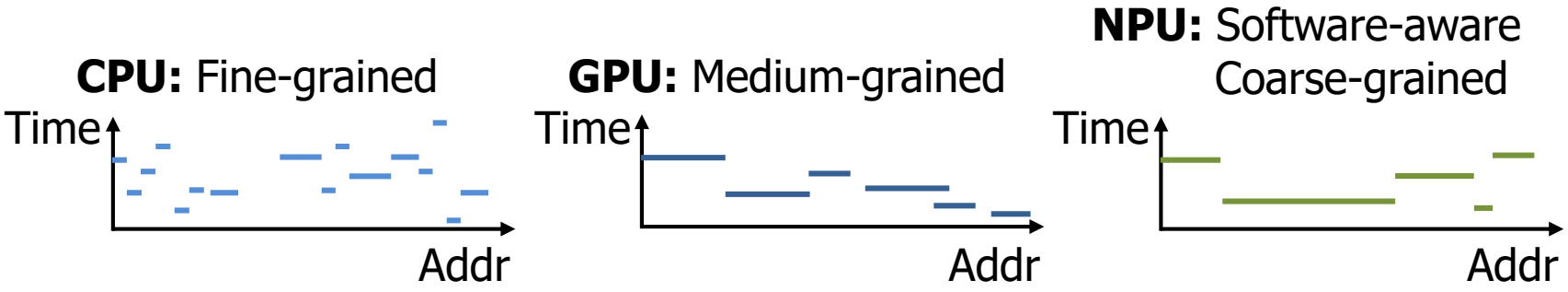


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**This study constructs a unified memory protection scheme with integrity tree optimization for heterogeneous processors**

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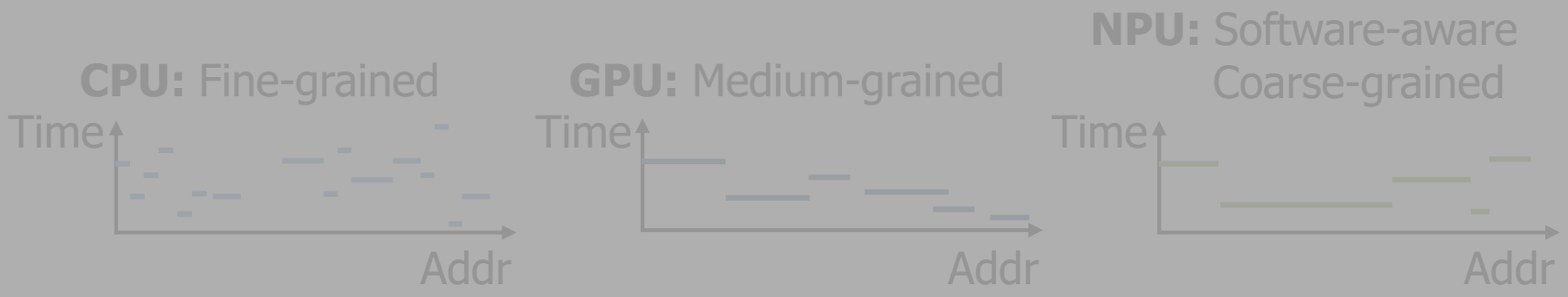


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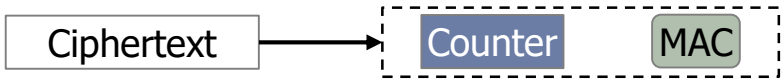

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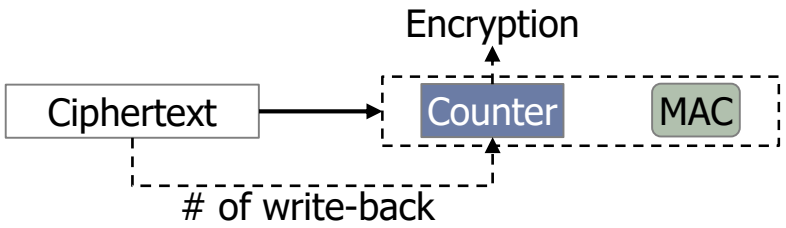

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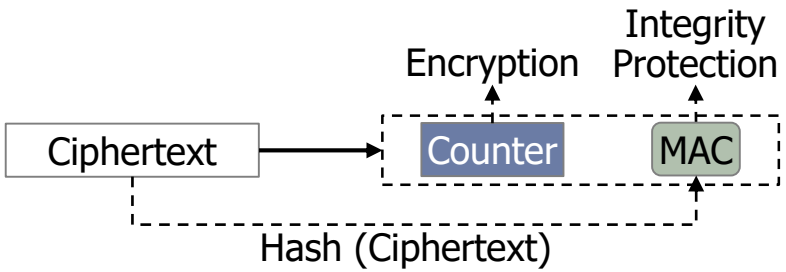

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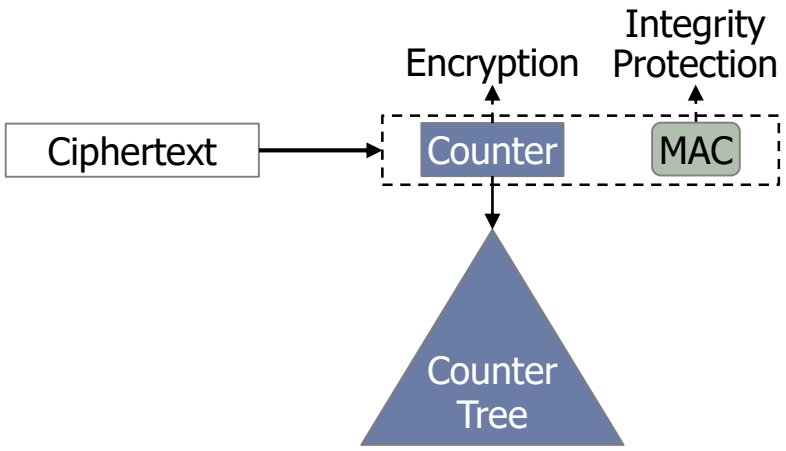

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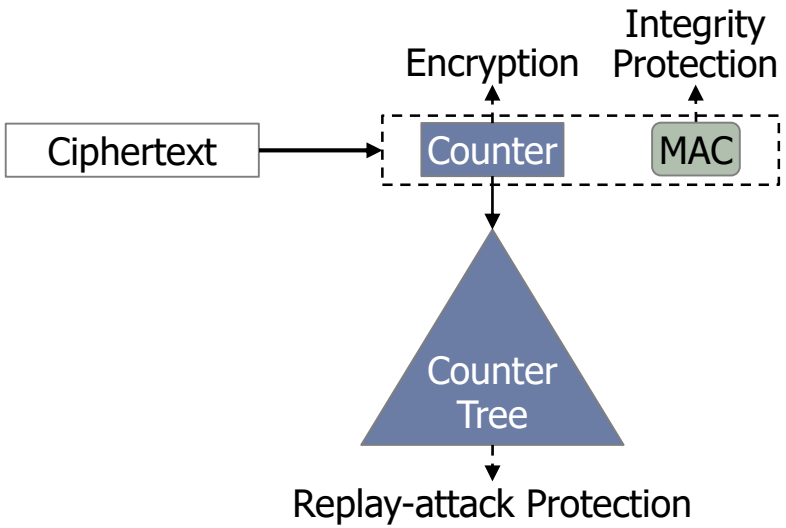

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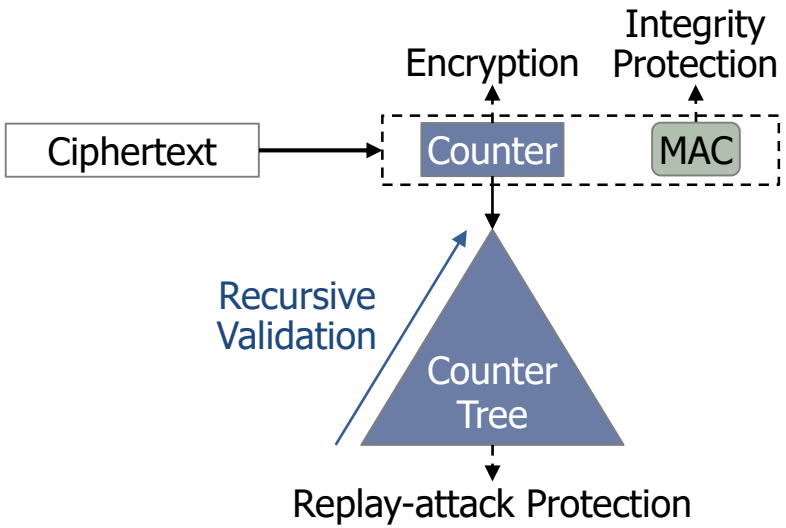

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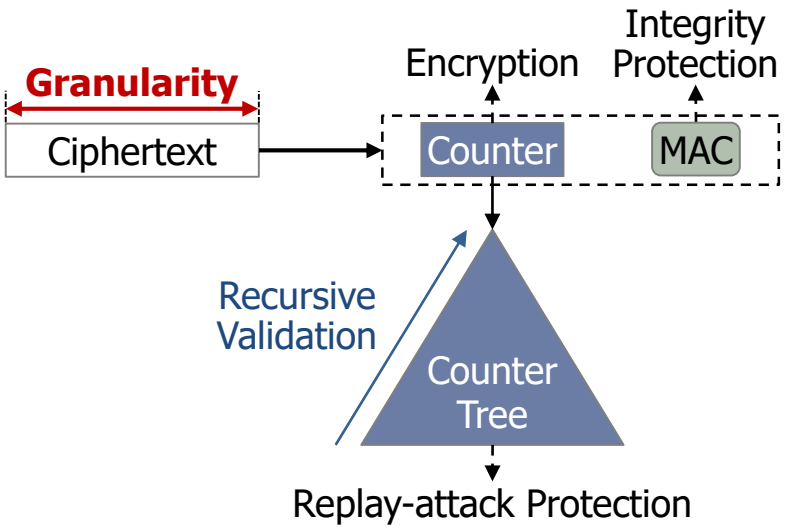

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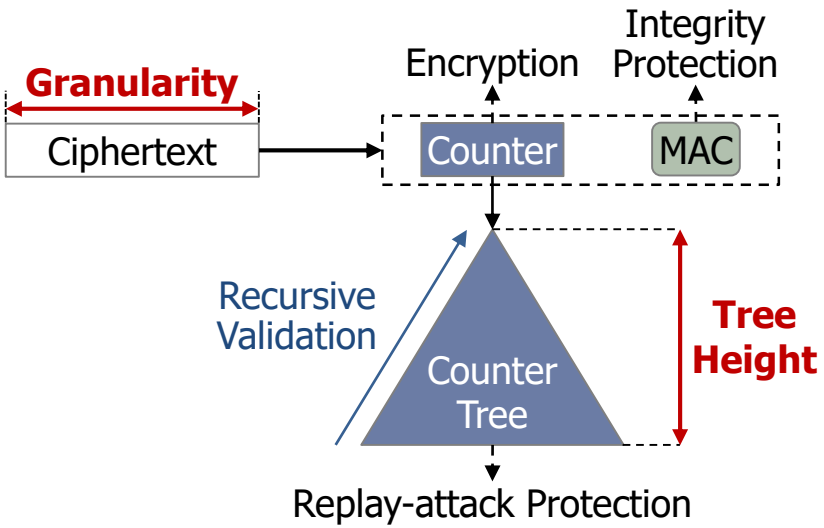

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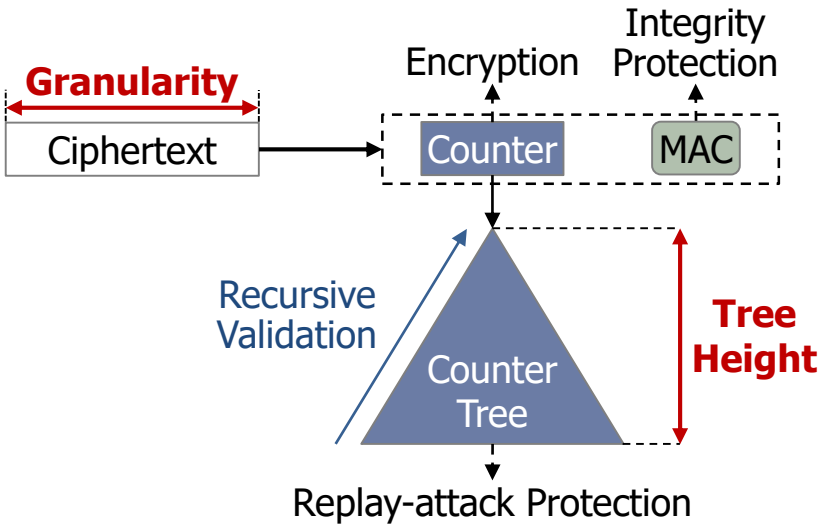


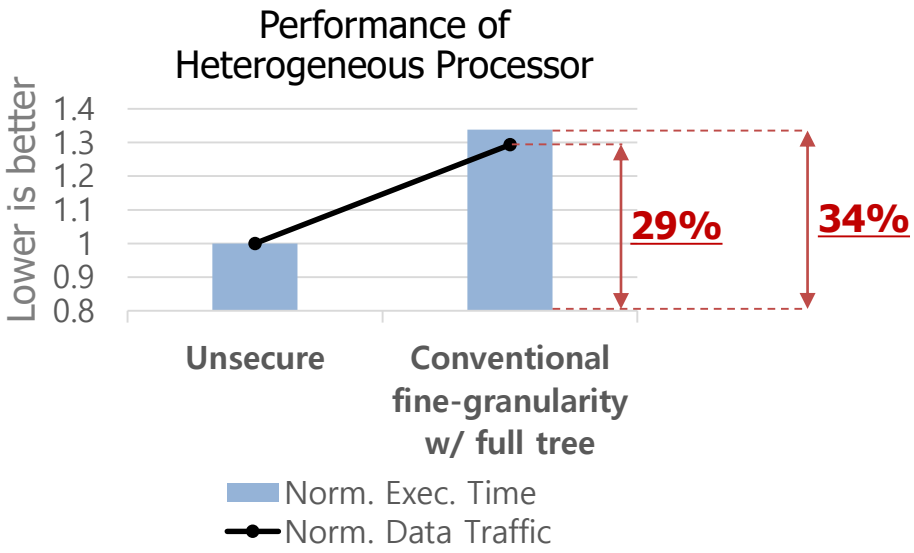

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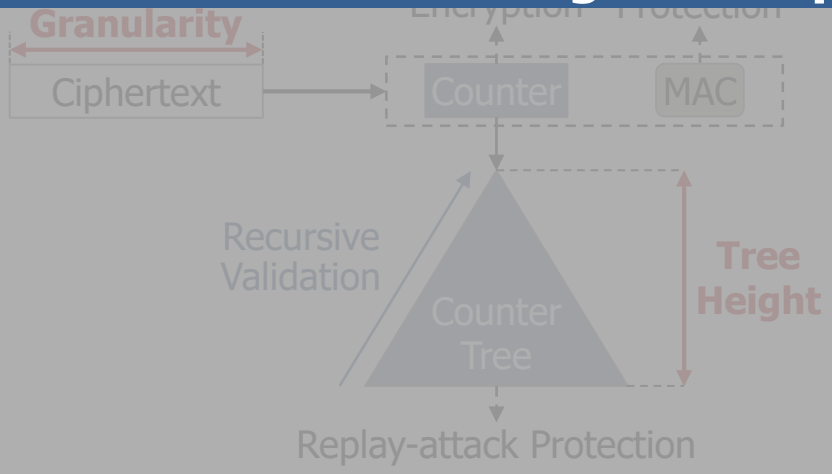
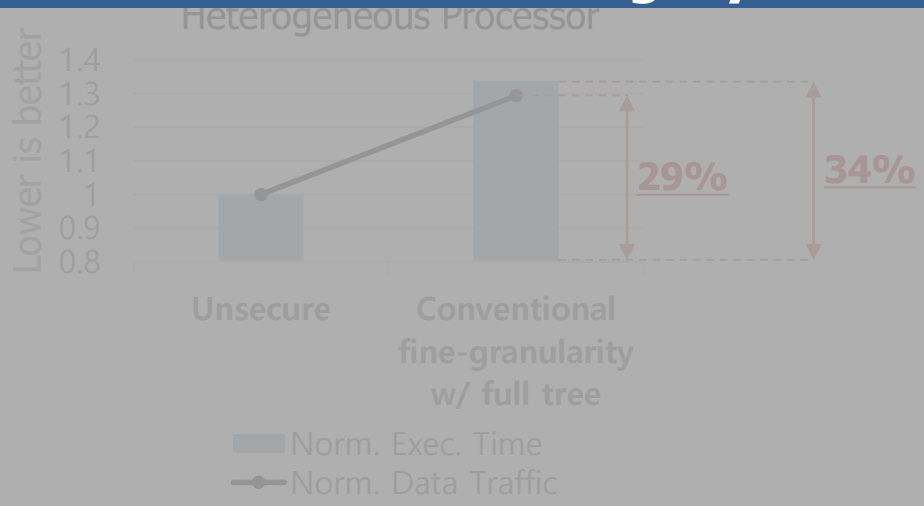
**Significant overhead caused by the conventional 64B-granular protection with a full integrity tree**



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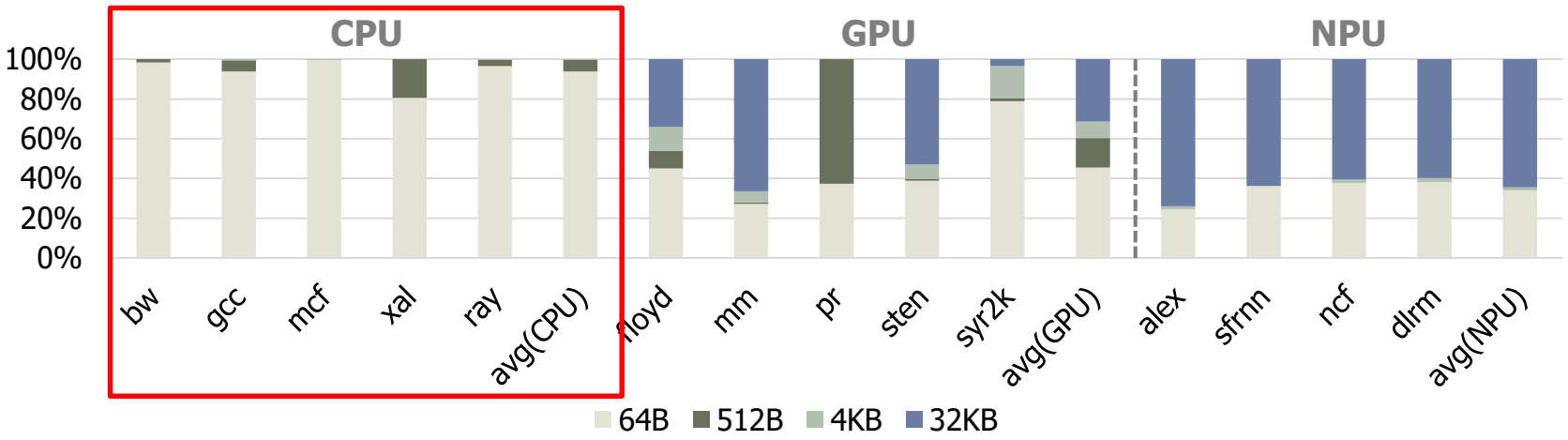

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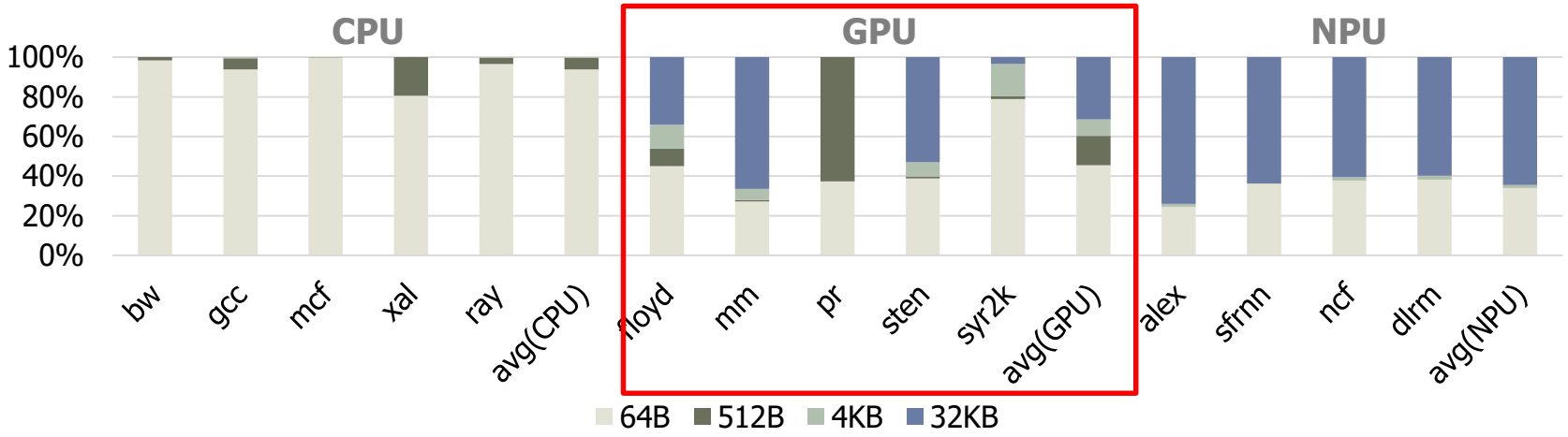

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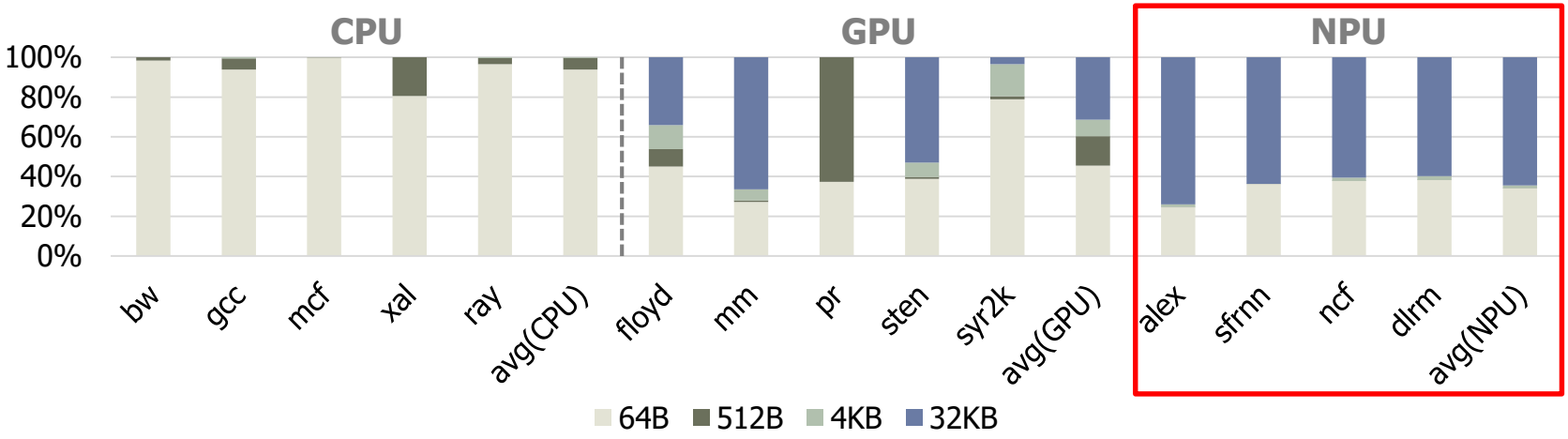

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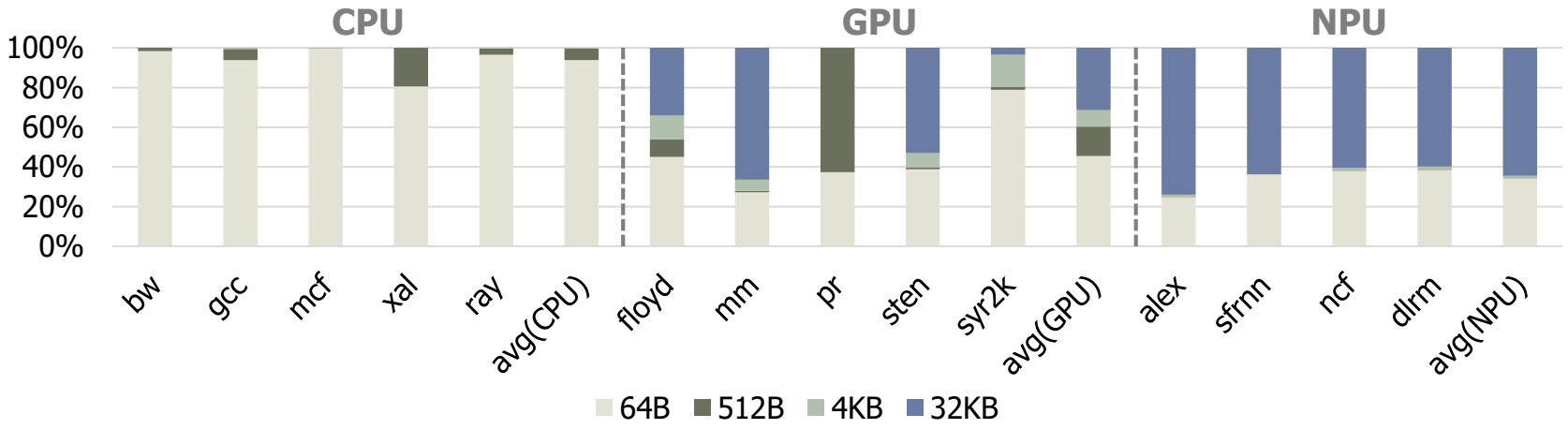


**Matching security granularity to access granularity**

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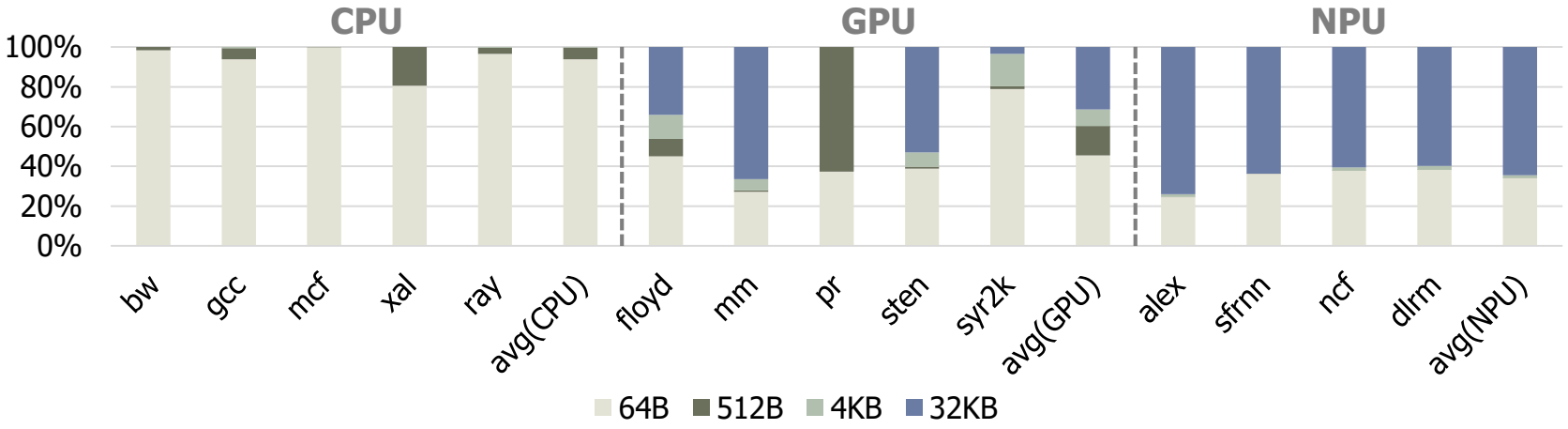
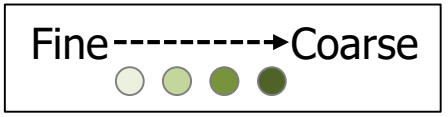
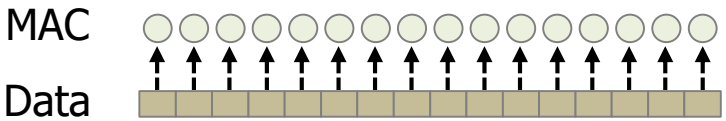



**Matching security granularity to access granularity**
**→ Requirement: Multi-granularity for MACs and counters**

# Multi-granular MAC




**Conventional Fine-granular MAC**



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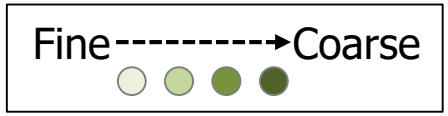


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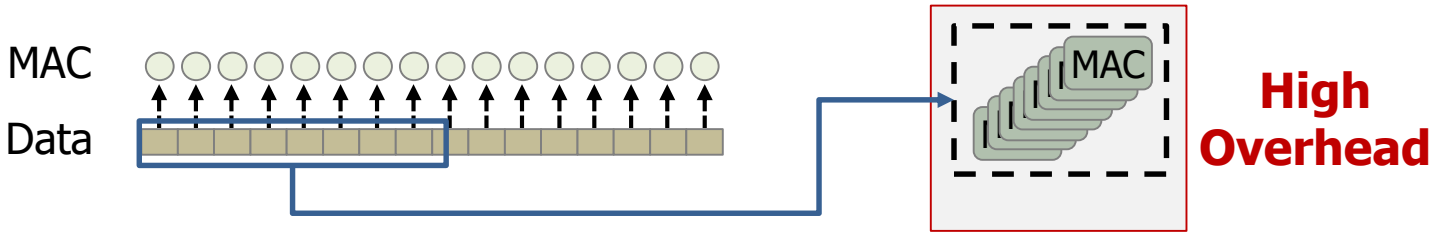

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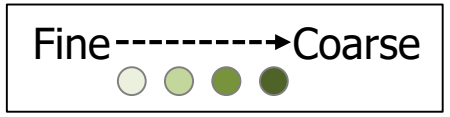


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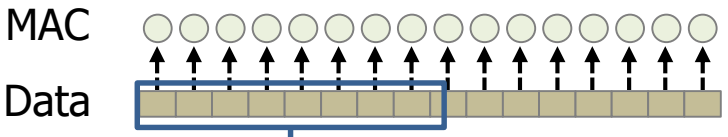
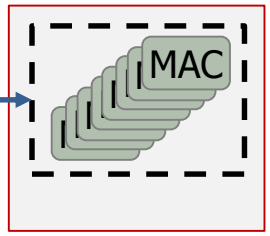
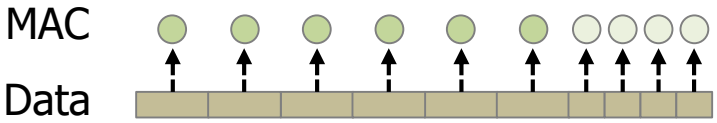



**High Overhead**

**Dual-granular MAC** [1]

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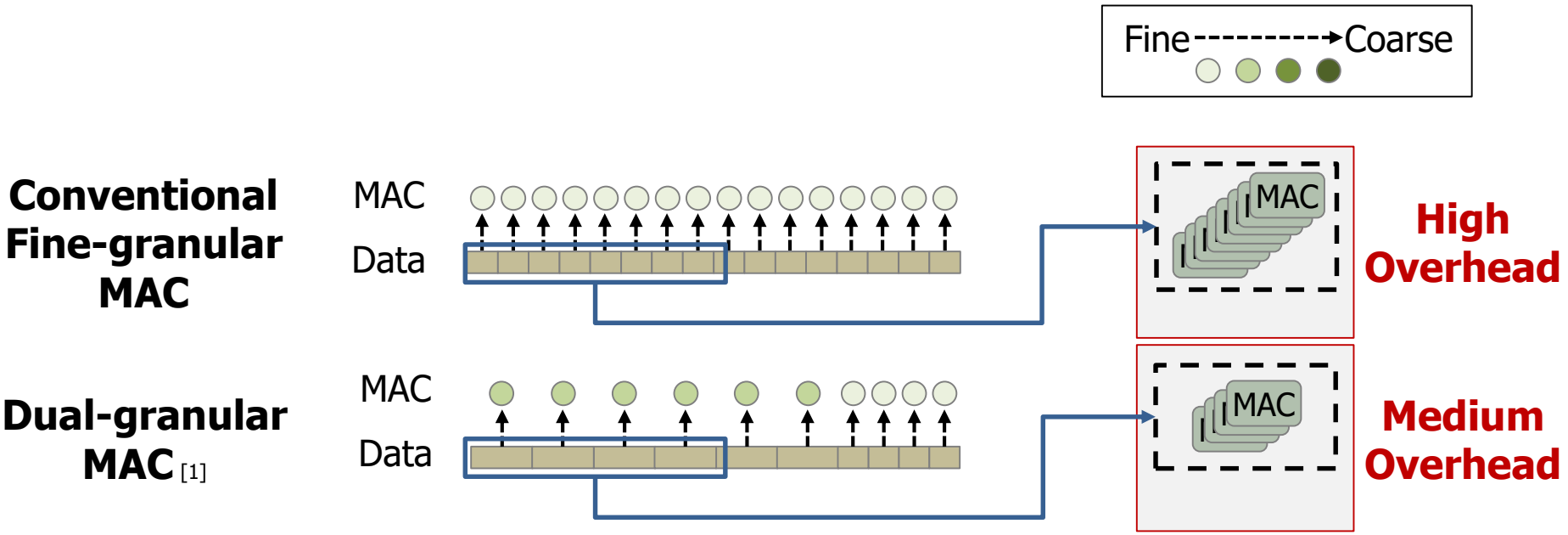


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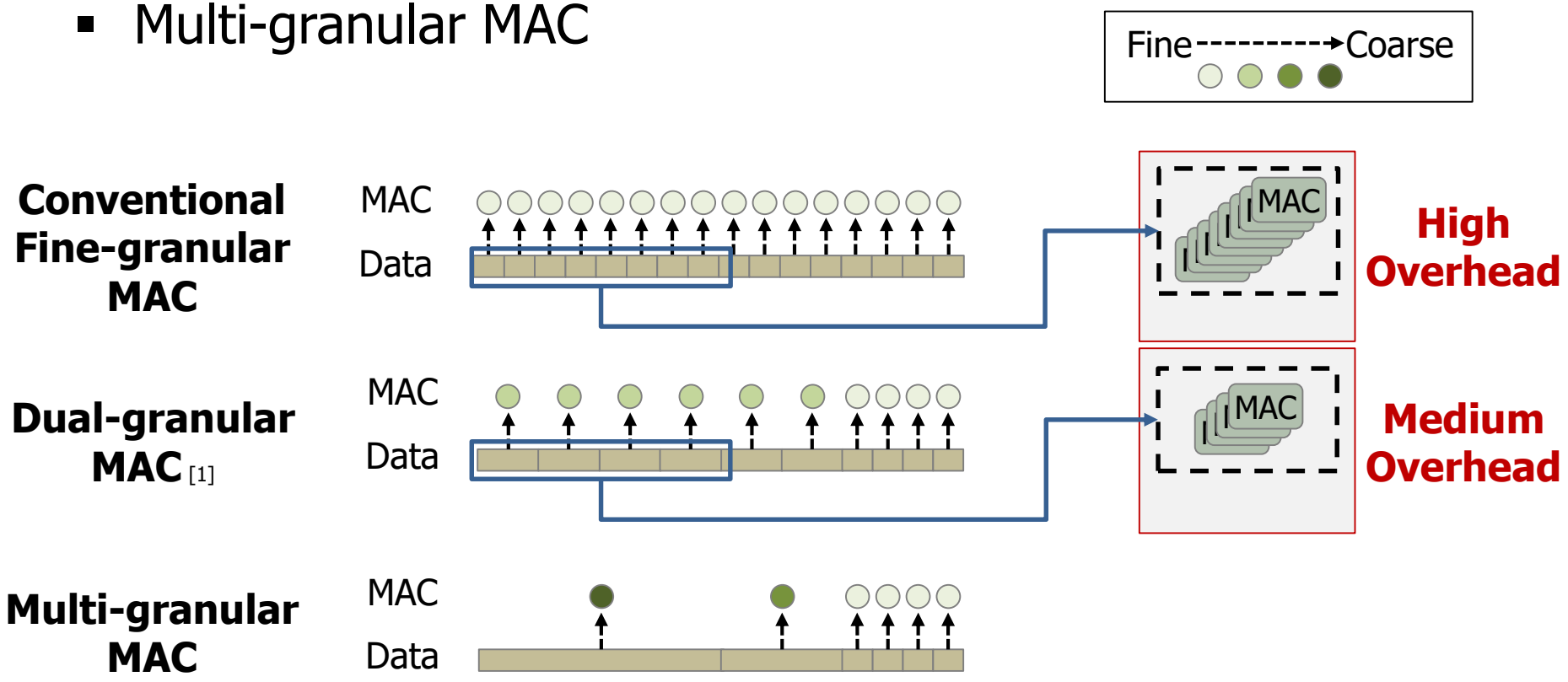


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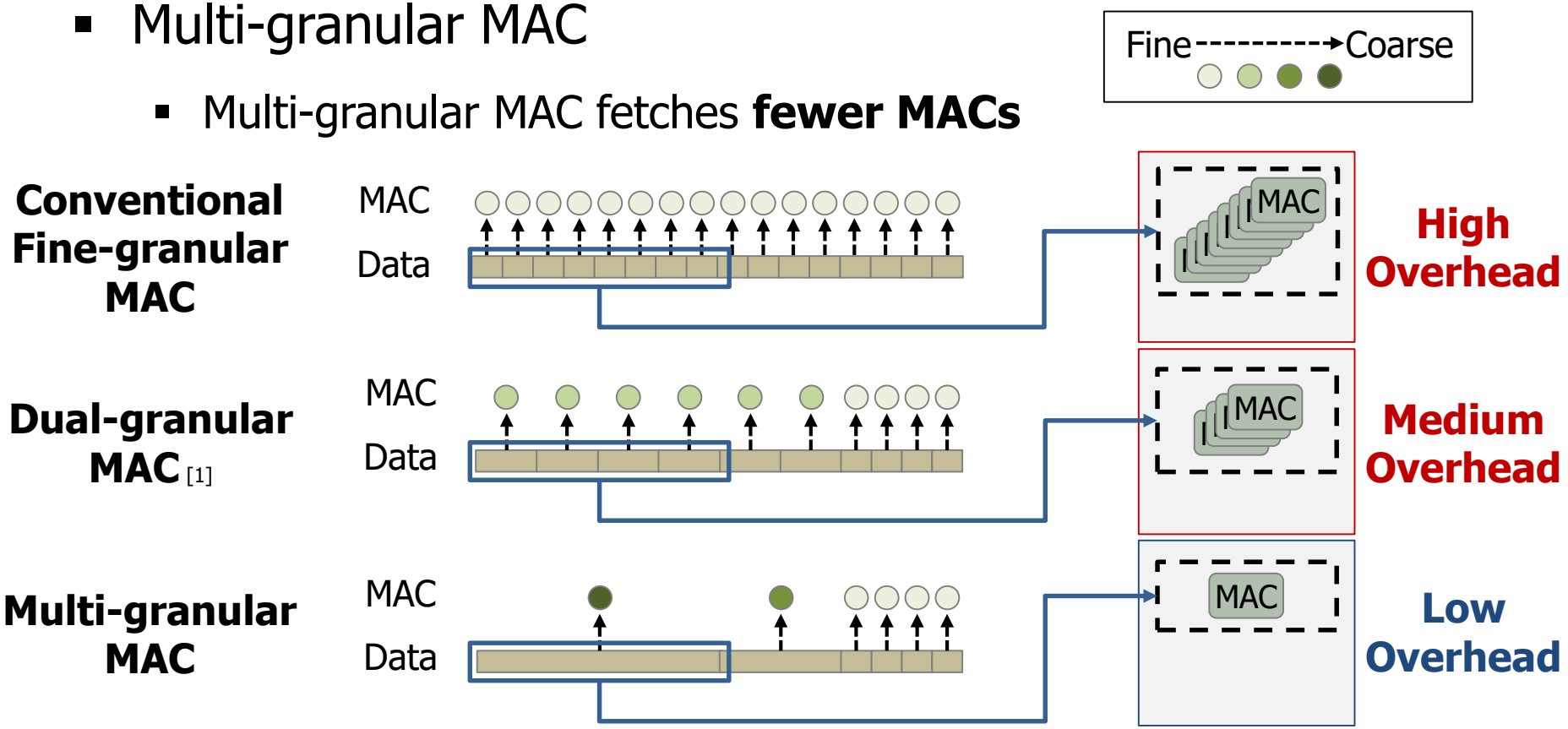


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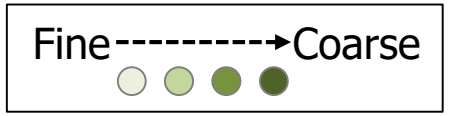


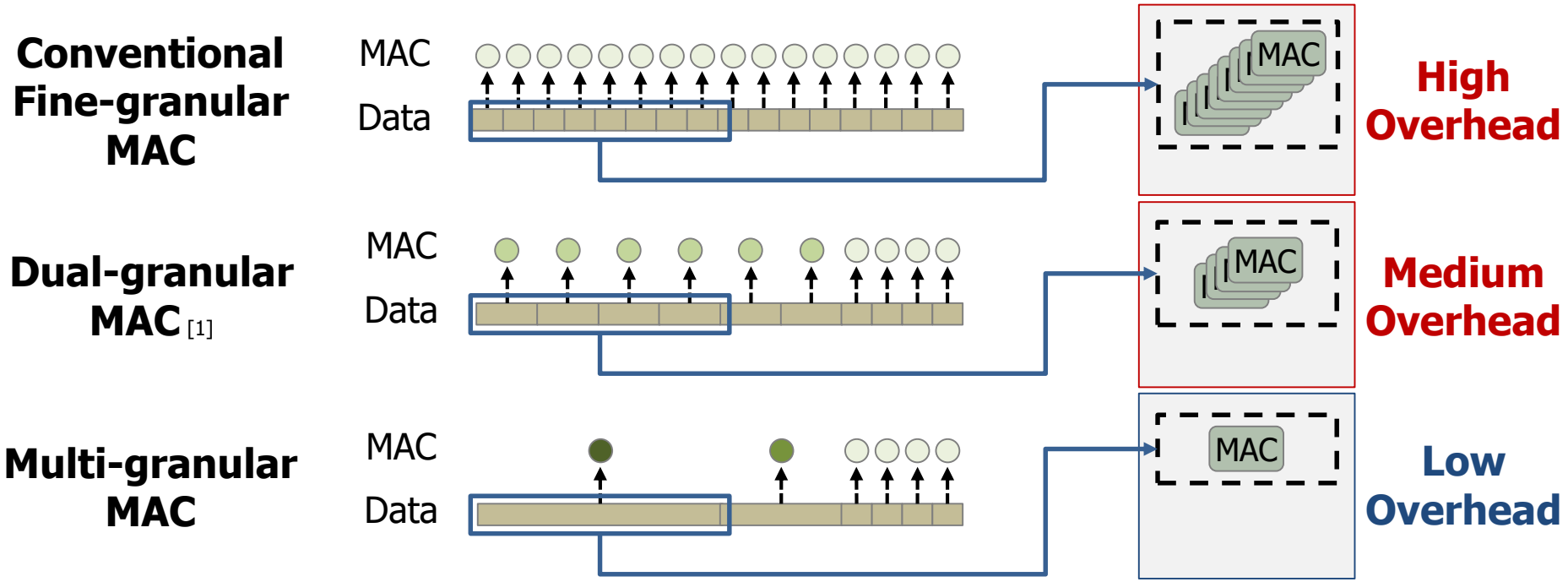


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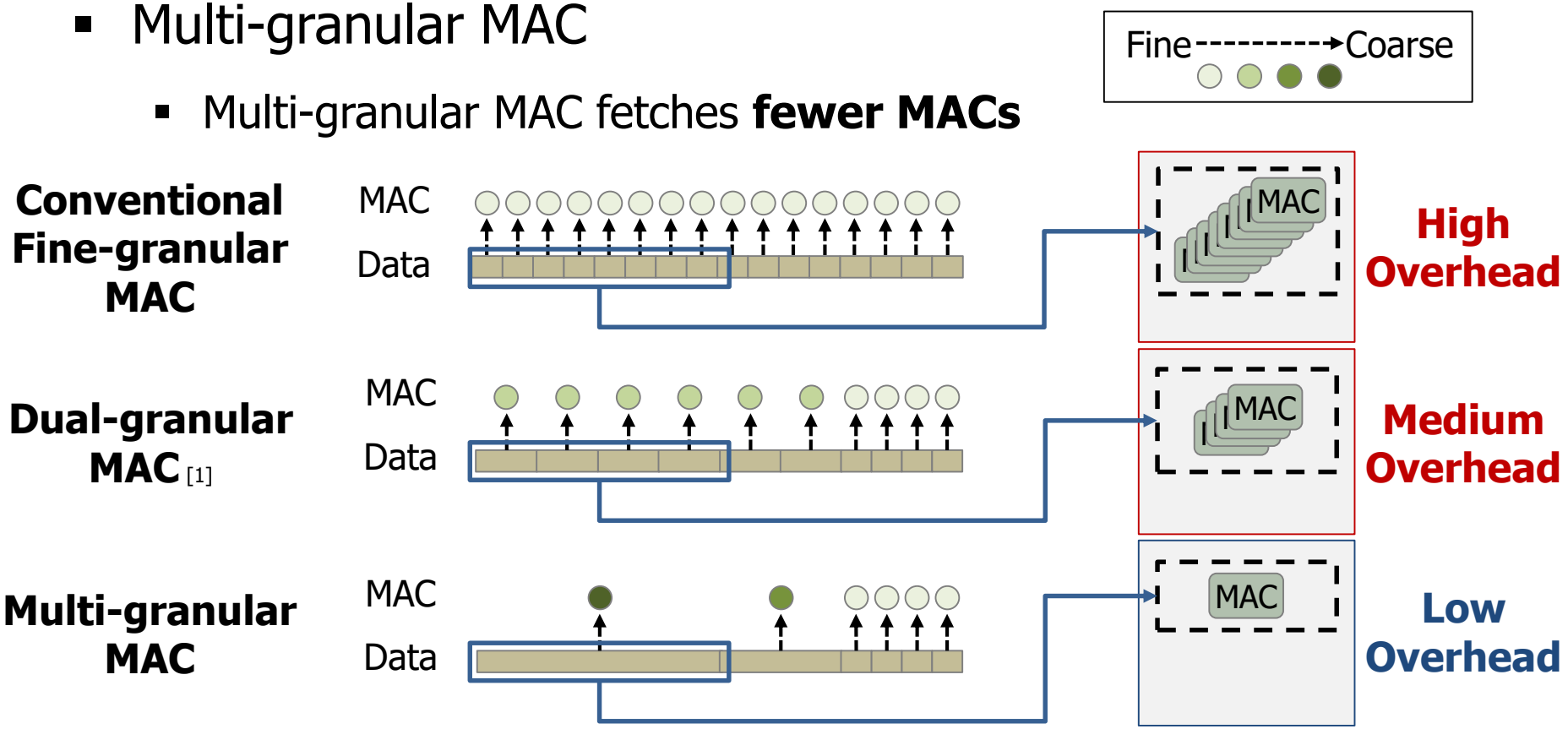


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**What about multi-granular counters?**

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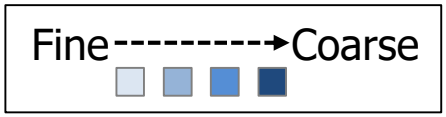
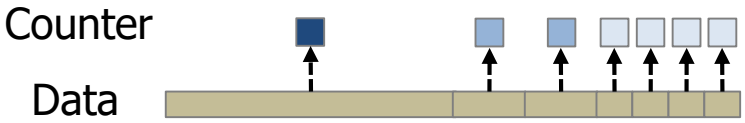


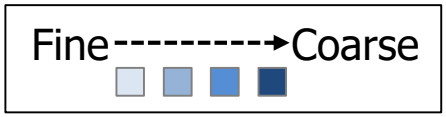

**Common Counters** [1]




[1] Common Counters: Compressed Encryption Counters for Secure GPU Memory (HPCA 2021)

# Prior Multi-granular Counter

- Due to **integrity tree**, prior studies bypass integrity tree under specific conditions.

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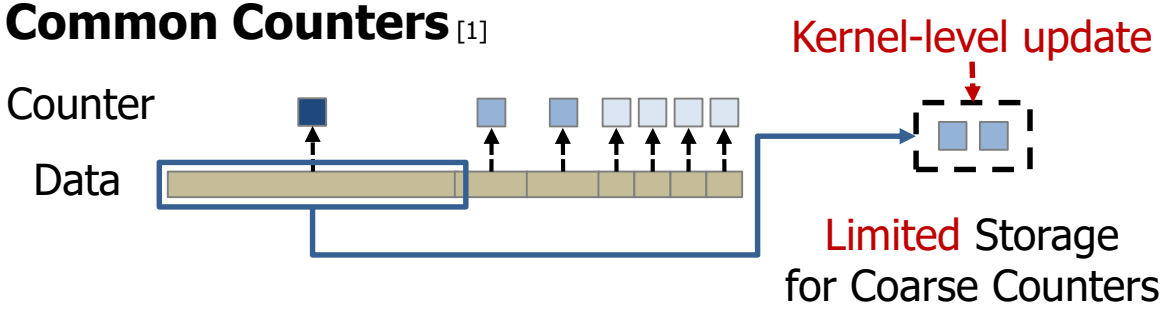


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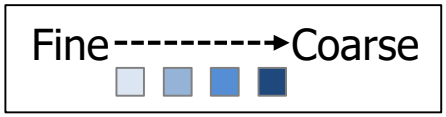


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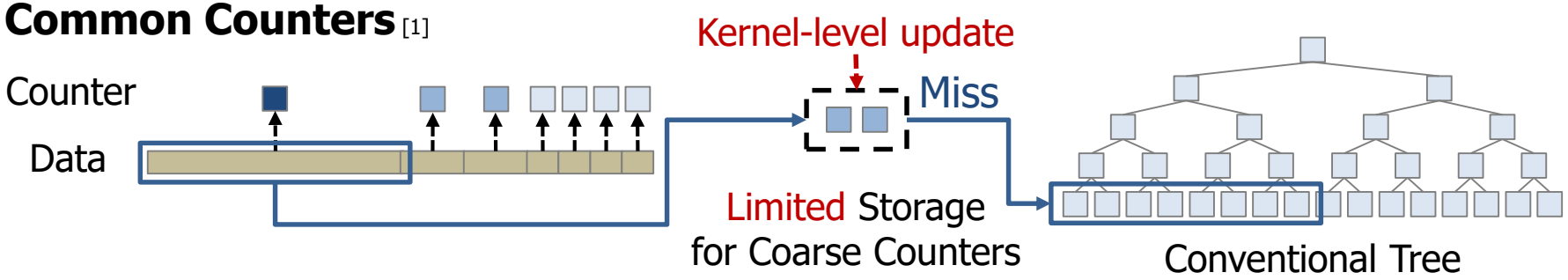


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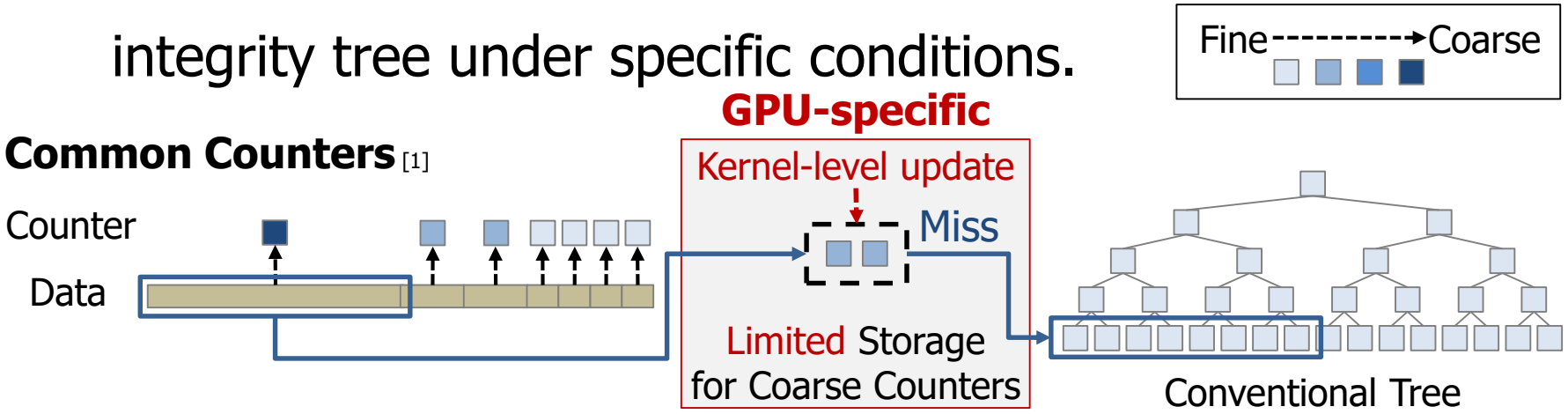


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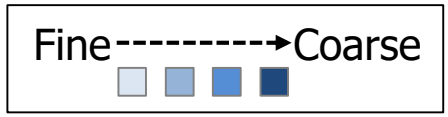
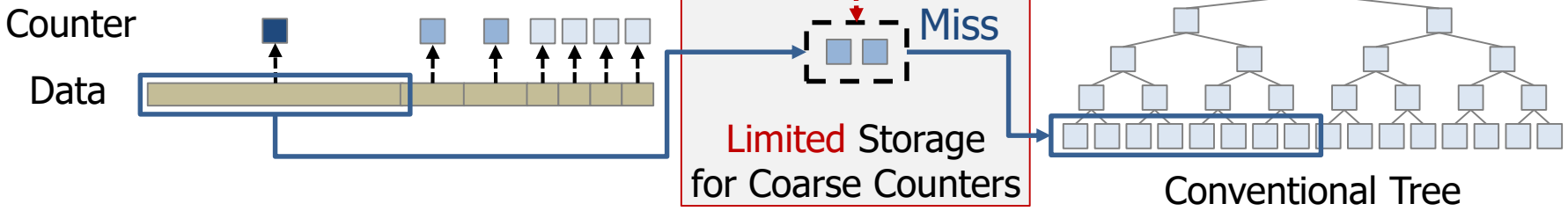
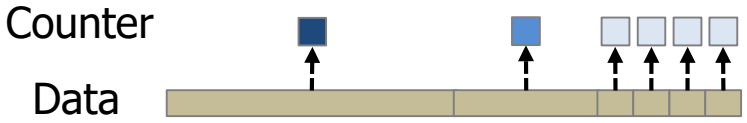



**GPU-specific**

**Common Counters** [1]




**S/W-managed Studies** [2-5]

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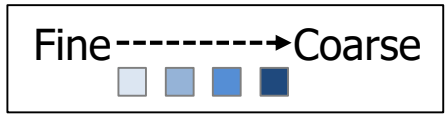


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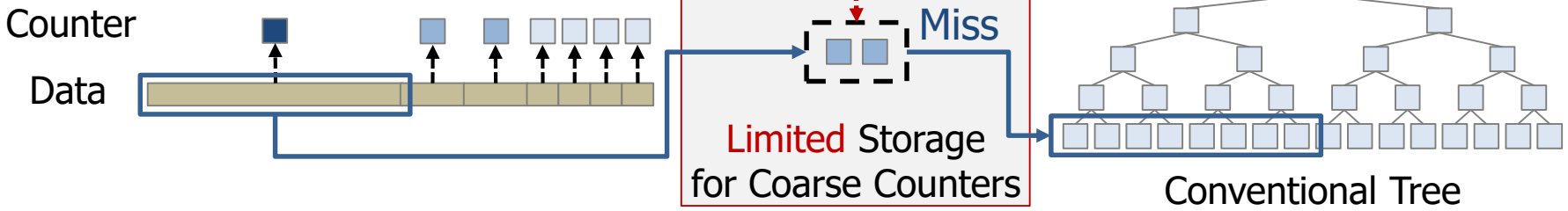


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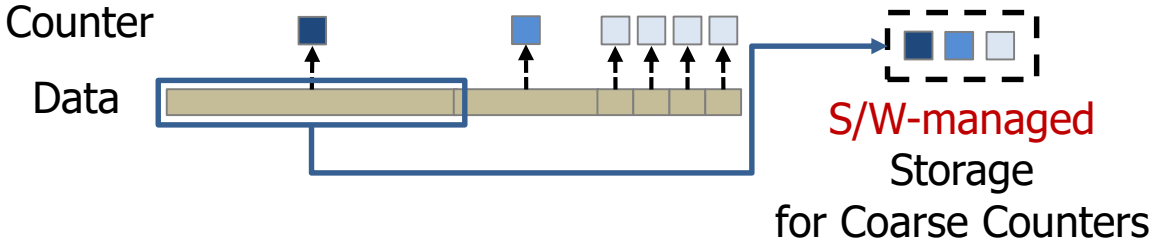


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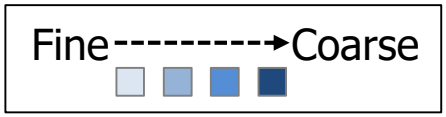


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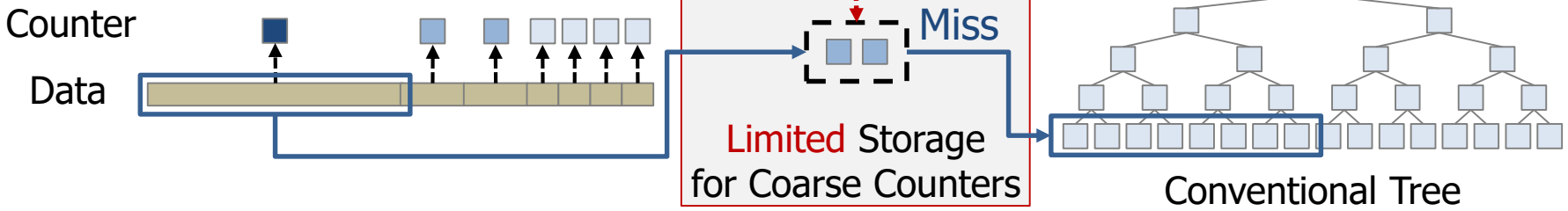


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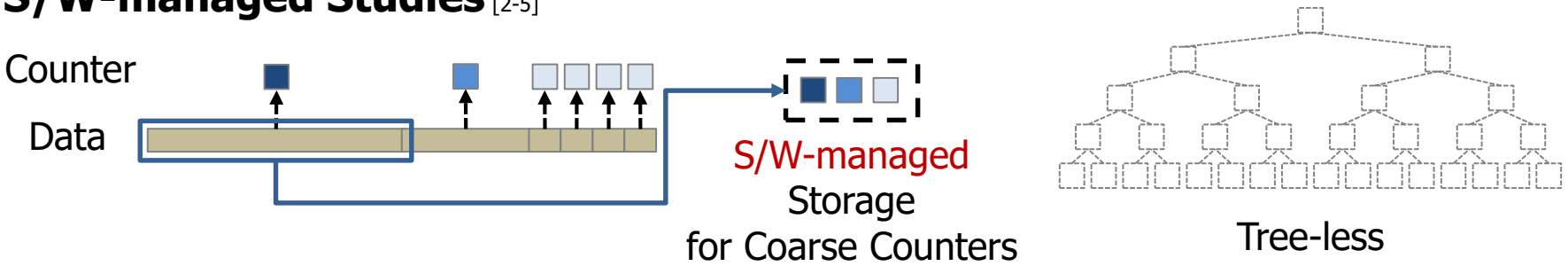


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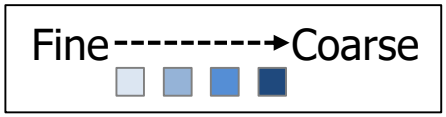


**GPU-specific**

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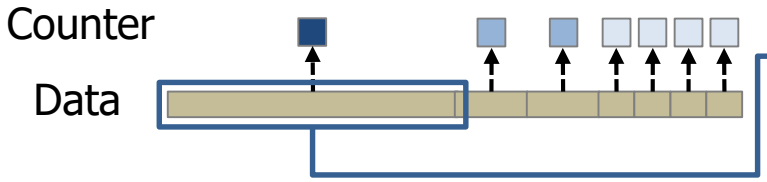
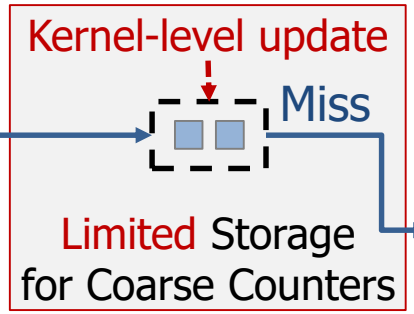
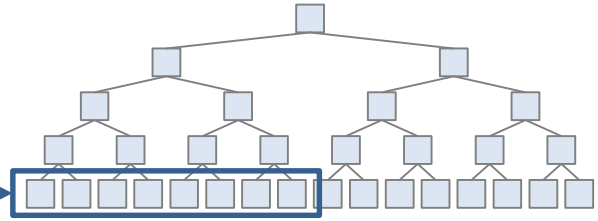


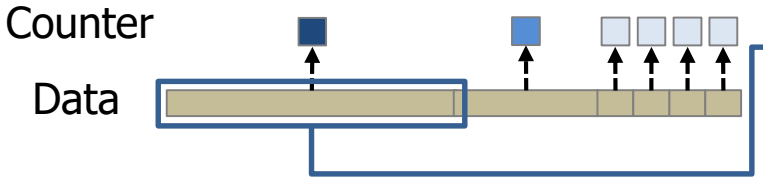



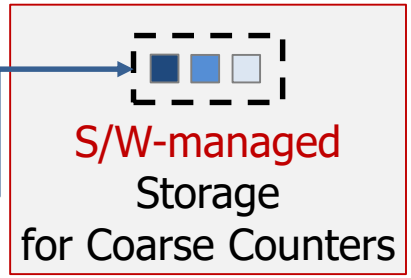



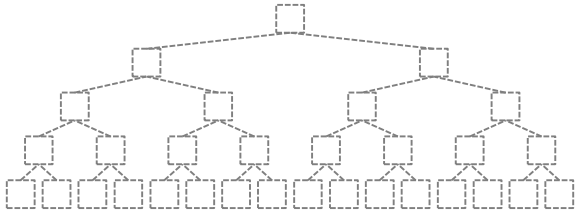
Conventional Tree

**S/W-managed Studies** [2-5]

**ML-specific**



Tree-less

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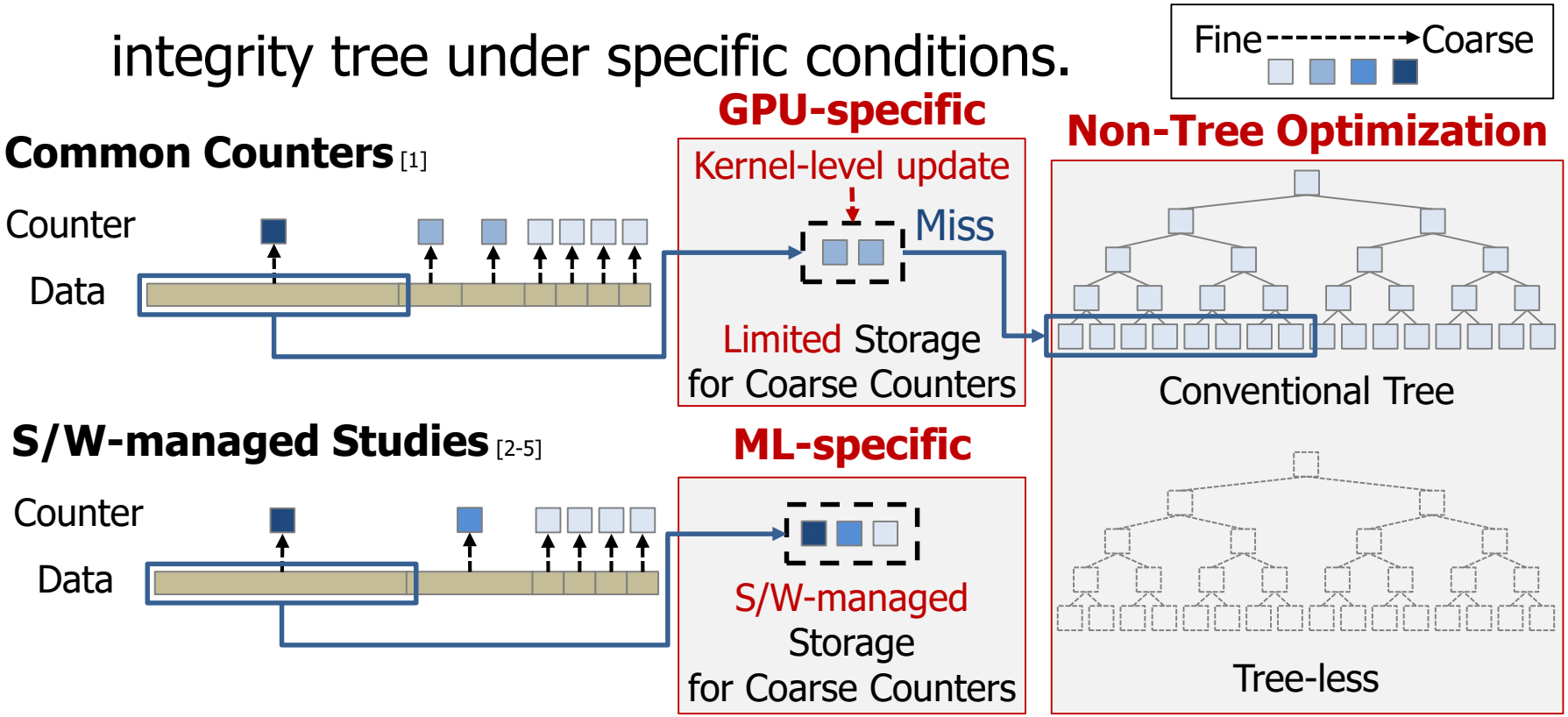



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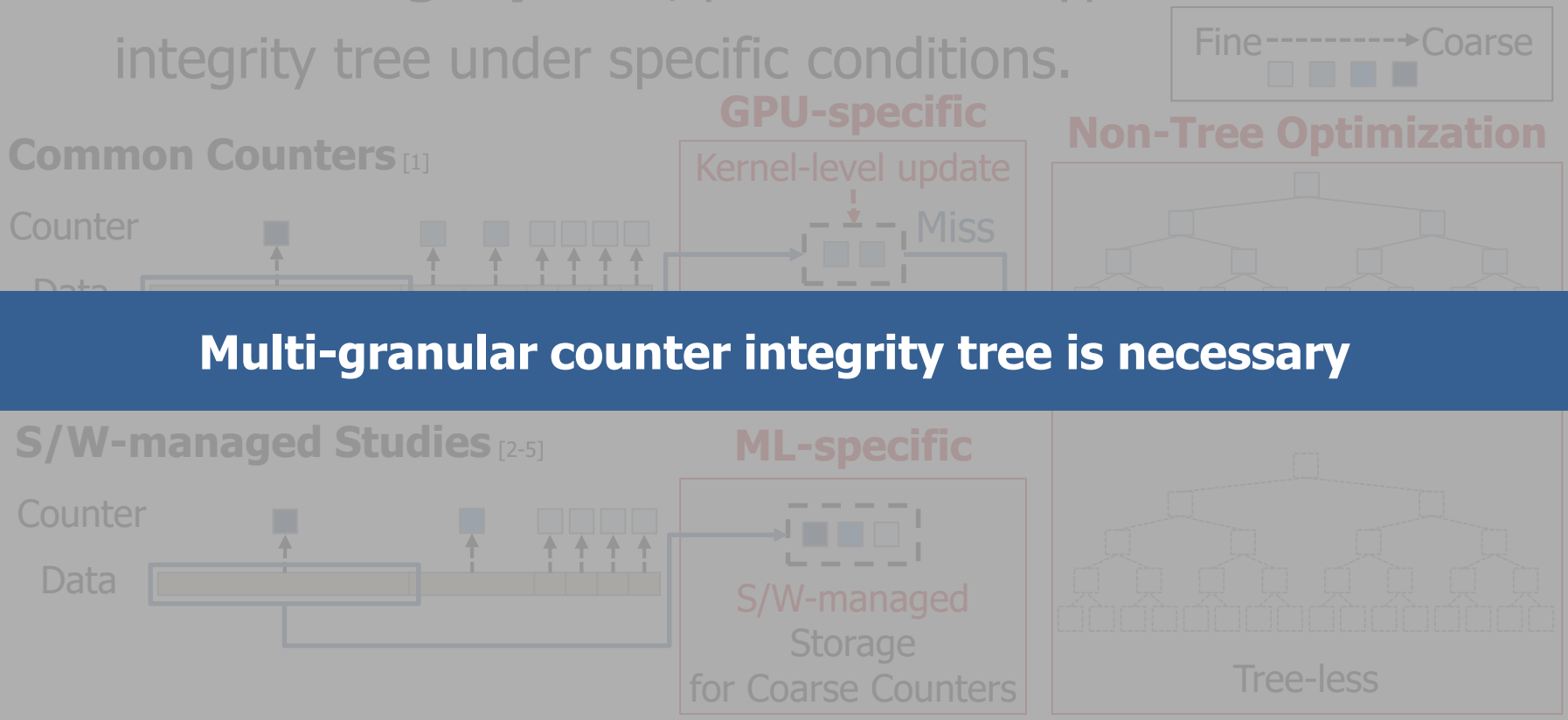


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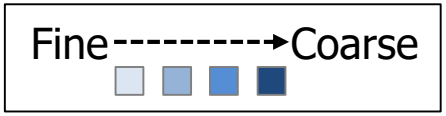
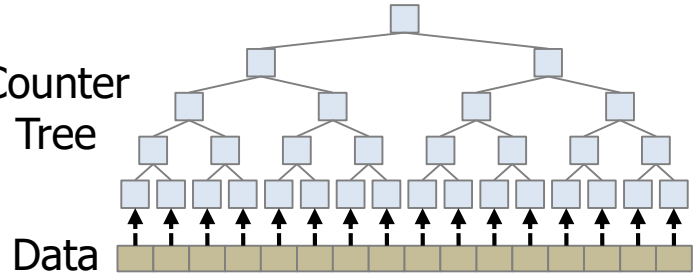
# Multi-granular Counter Integrity Tree




**Conventional Fine-granular Tree**



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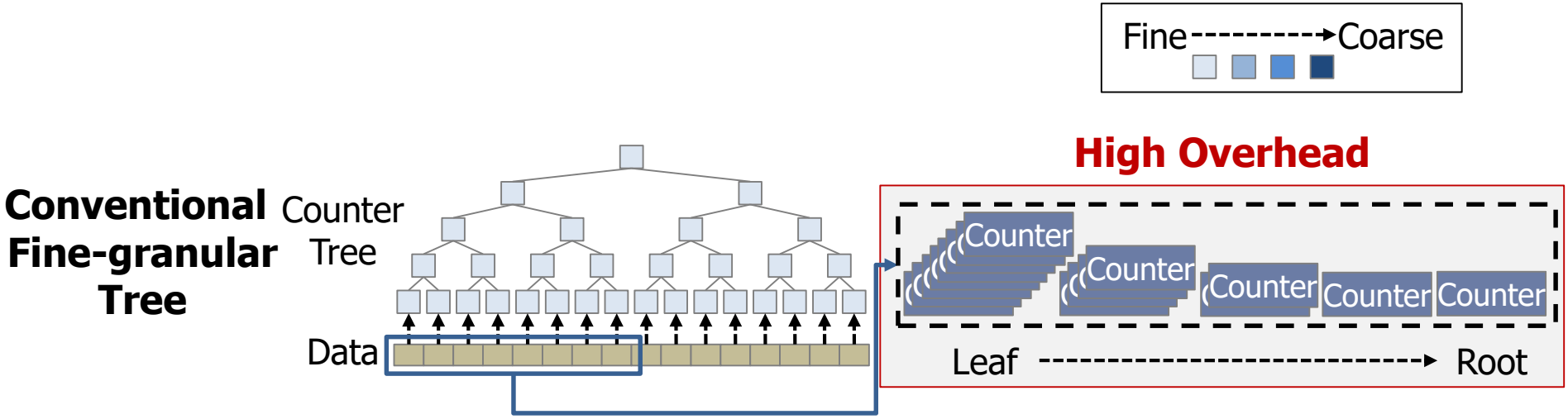

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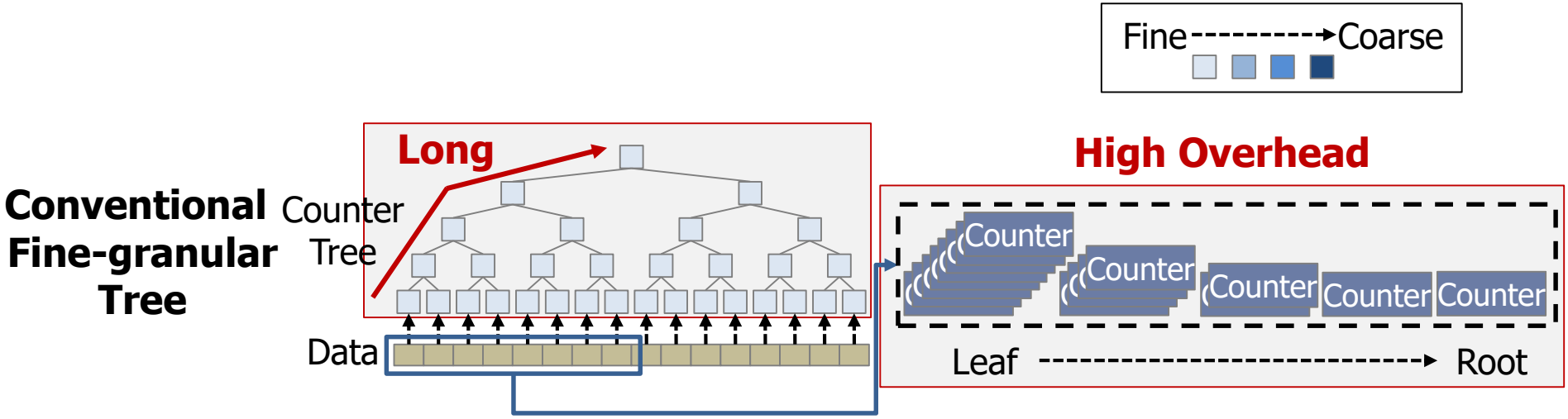
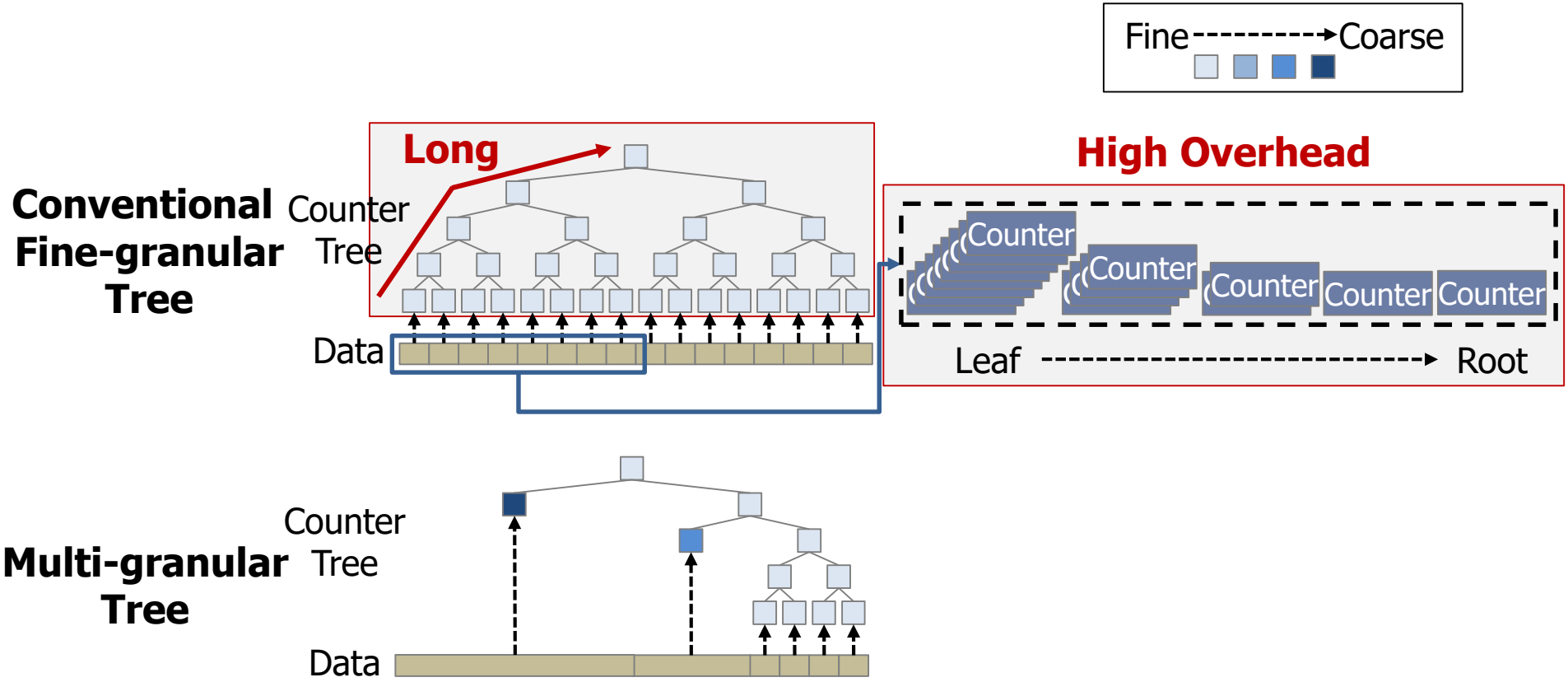


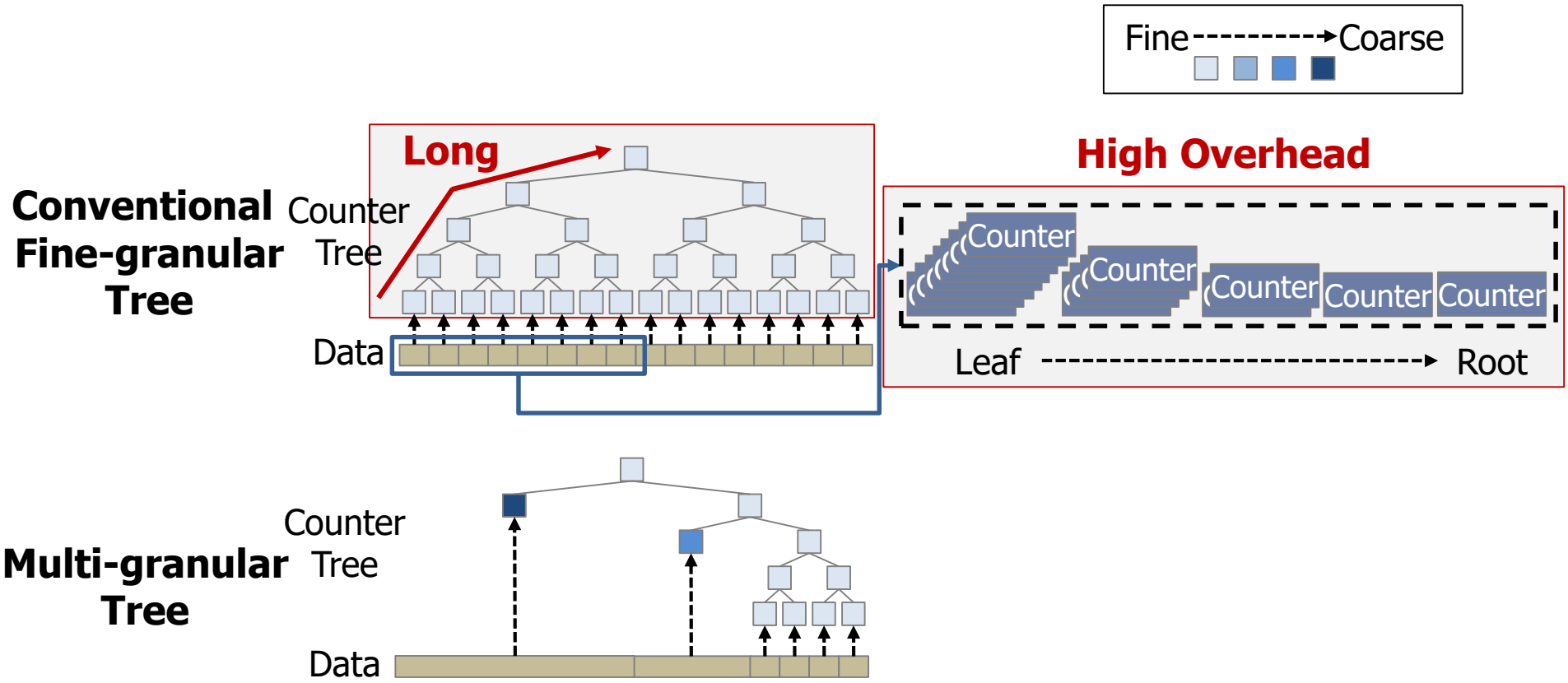
# Multi-granular Counter Integrity Tree

- Multi-granular tree



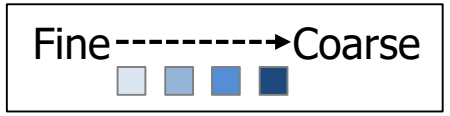
# Multi-granular Counter Integrity Tree

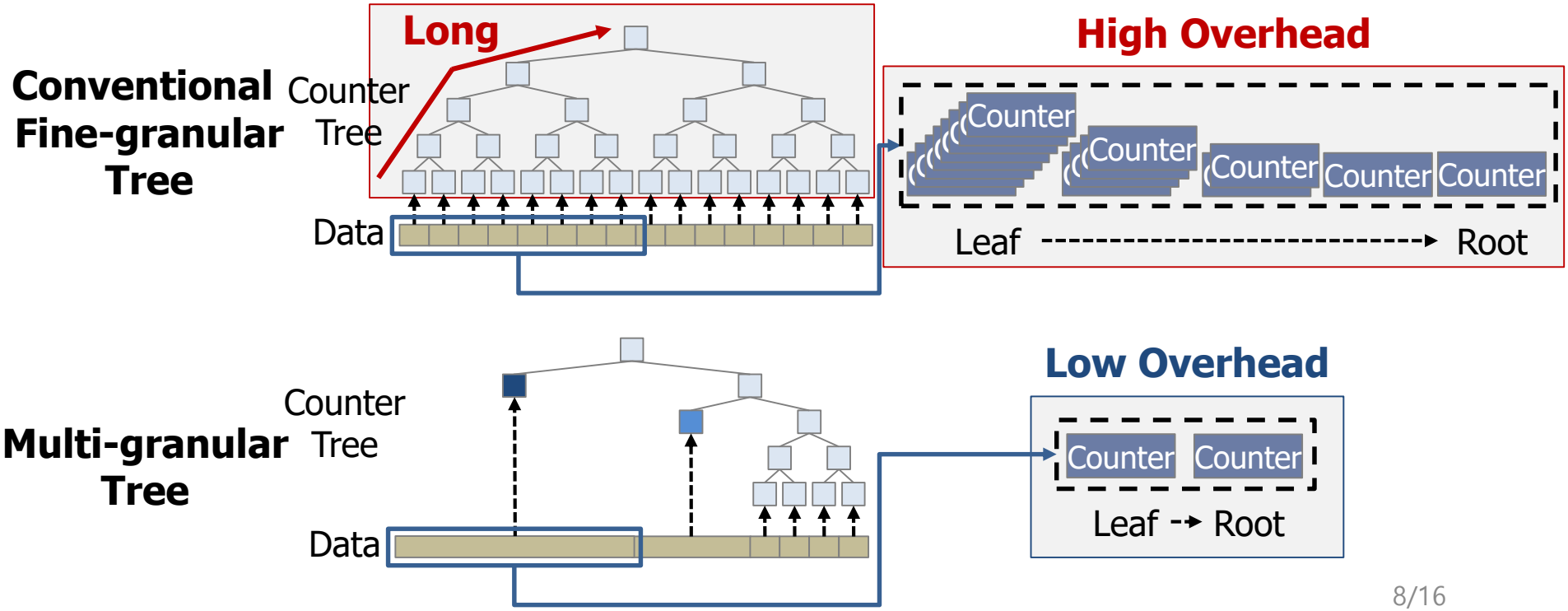
- Multi-granular tree
  - Counters w/ varying granularities are mapped to different levels



# Multi-granular Counter Integrity Tree

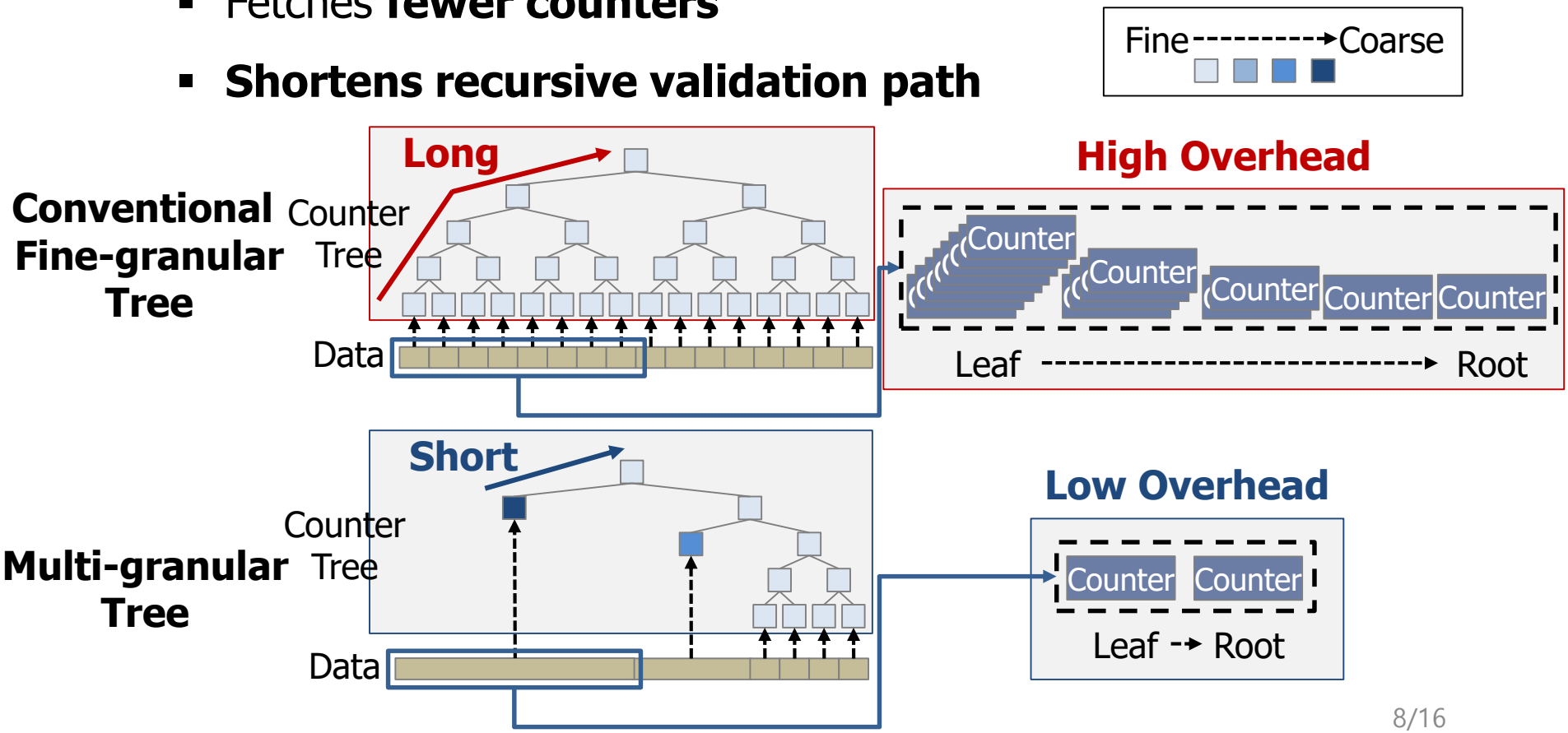
- Multi-granular tree
  - Counters w/ varying granularities are mapped to different levels
  - Fetches **fewer counters**



# Multi-granular Counter Integrity Tree

- Multi-granular tree
  - Counters w/ varying granularities are mapped to different levels
  - Fetches **fewer counters**
  - **Shortens recursive validation path**



# Multi-granular MAC&Tree

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- Multi-granular MAC&Tree
  - Dynamically supports multi-granular MACs and a counter tree

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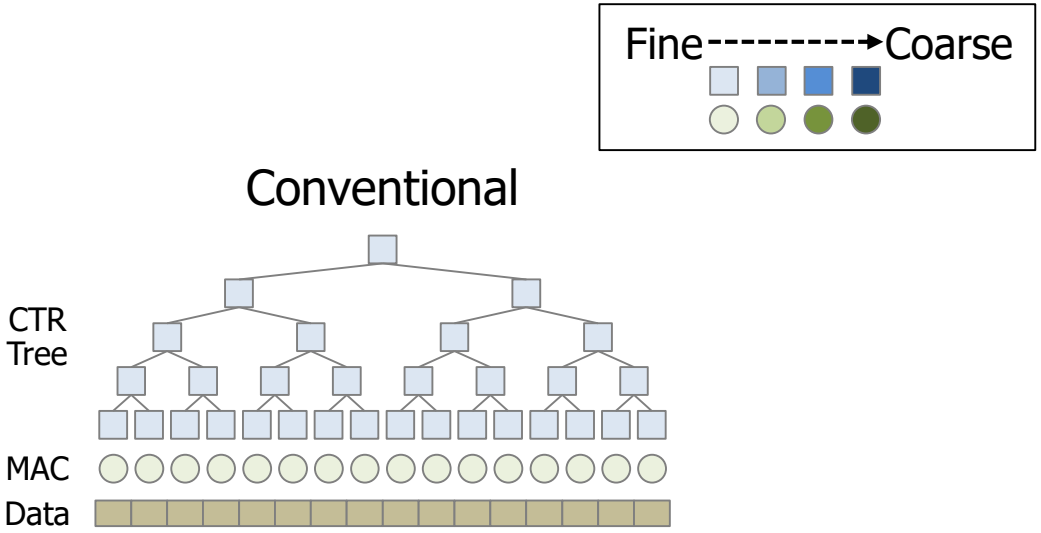

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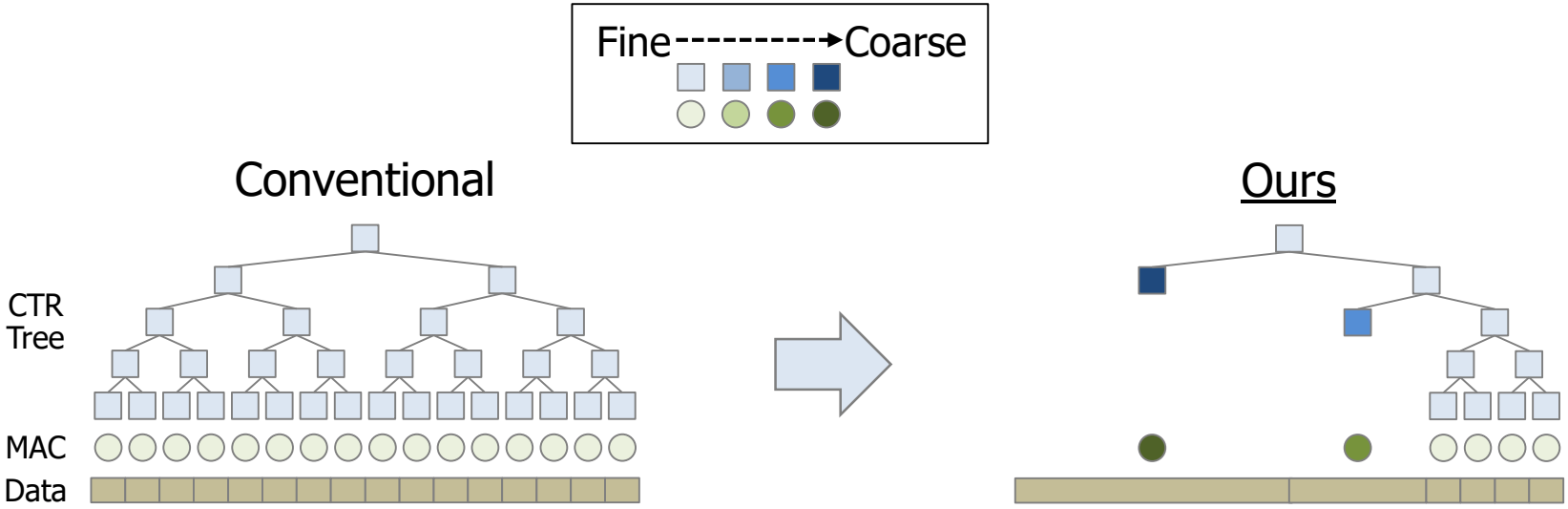
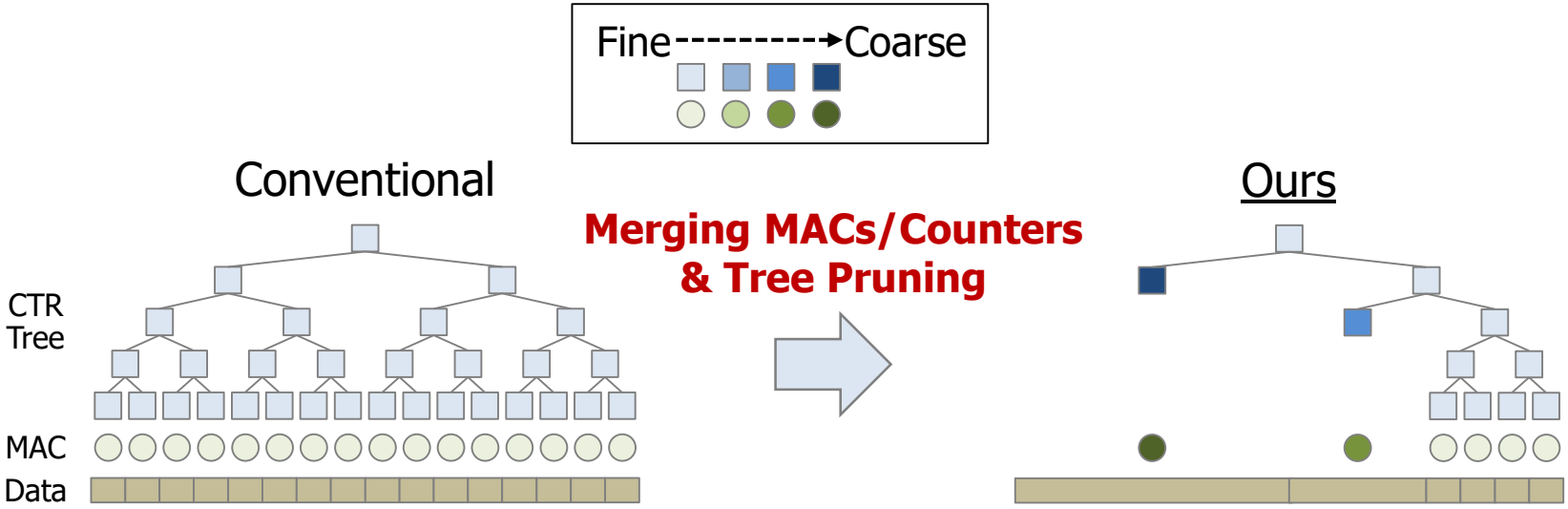


# Multi-granular MAC&Tree

- Multi-granular MAC&Tree
  - Dynamically supports multi-granular MACs and a counter tree
  - Key Idea: Merging MACs/counters & pruning a counter tree



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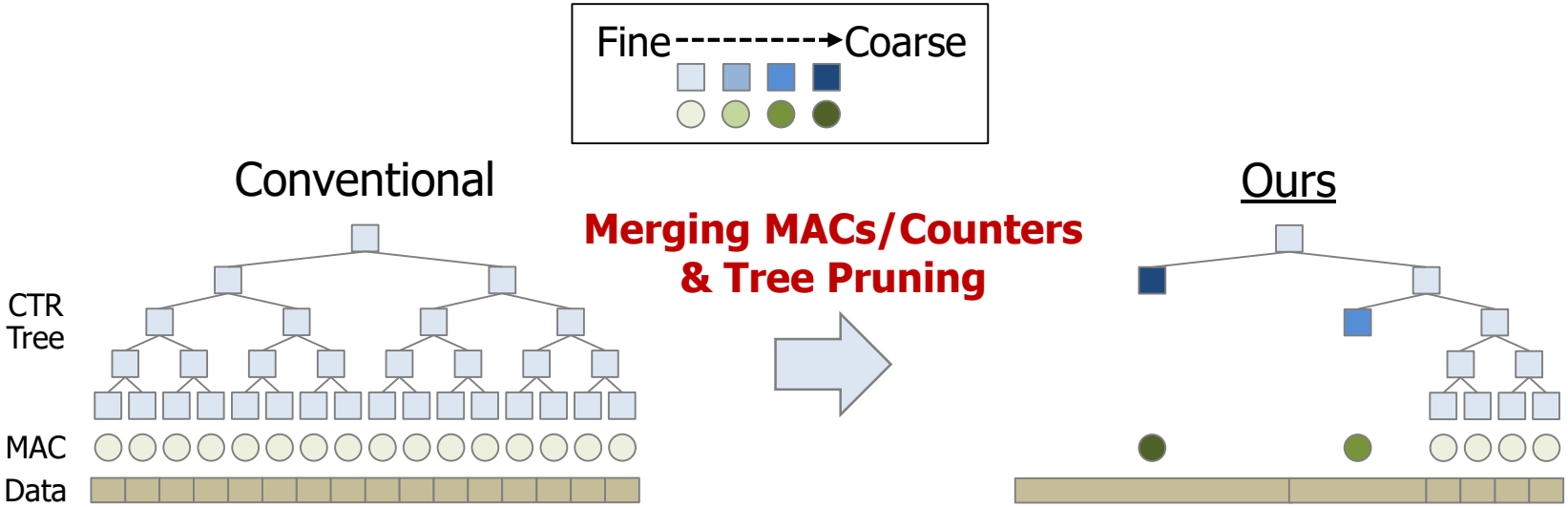


**1. How to dynamically detect granularity**

# Multi-granular MAC&Tree

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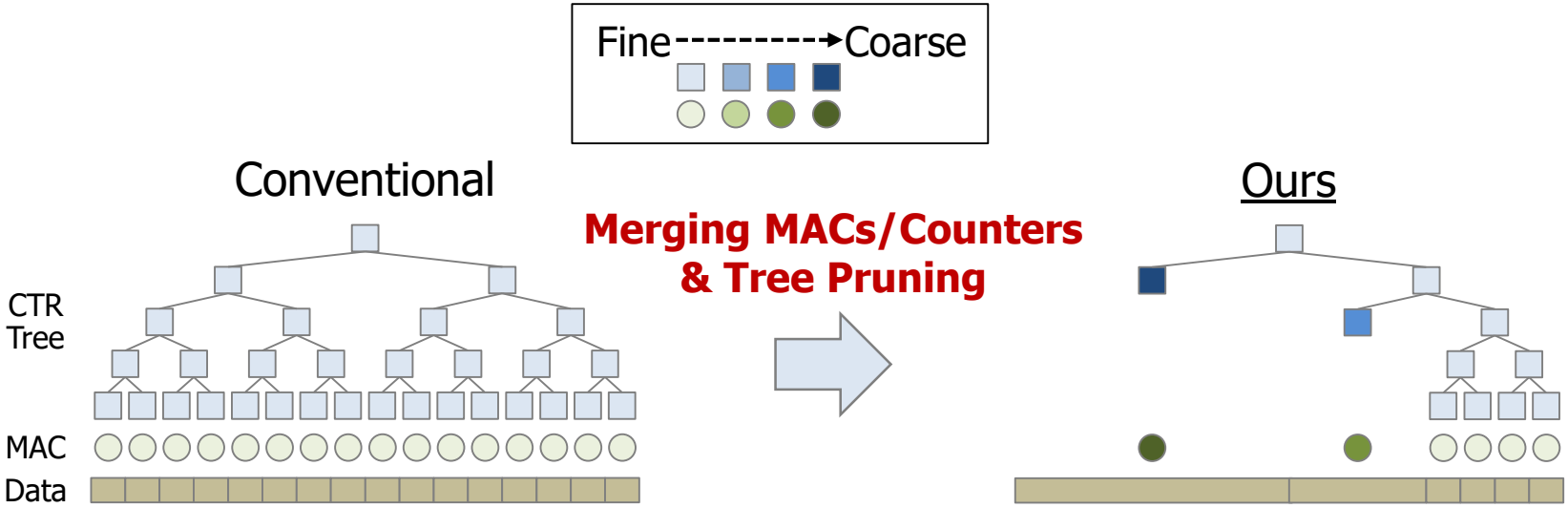
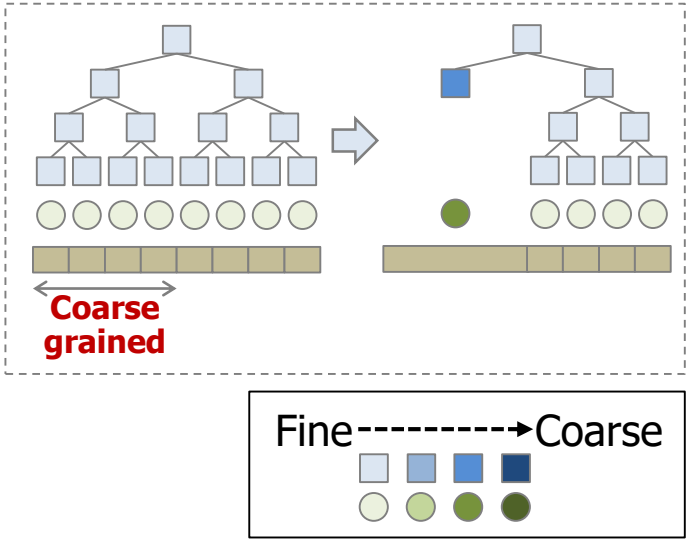
  - Dynamically supports multi-granular MACs and a counter tree
  - Key Idea: Merging MACs/counters & pruning a counter tree



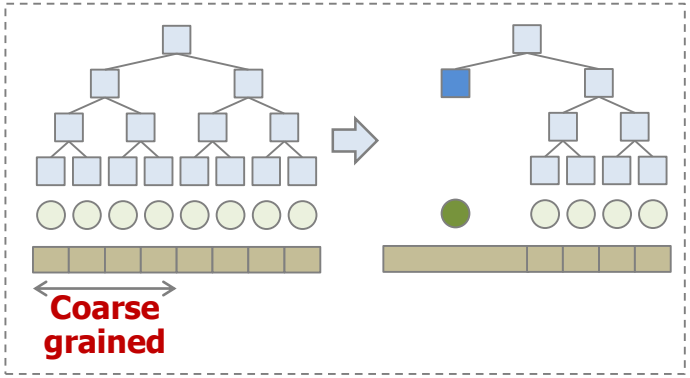

**1. How to dynamically detect granularity**
**2. How to switch granularity**

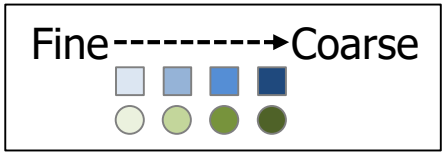
# Granularity Detection (Fine → Coarse)

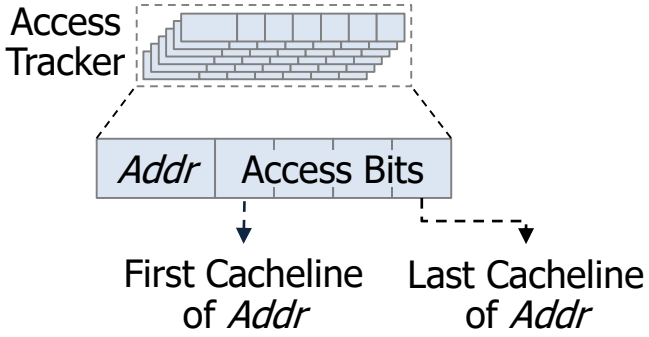


# Granularity Detection (Fine → Coarse)

- Access tracker
  - Records accessed addresses



# Granularity Detection (Fine → Coarse)

- Access tracker
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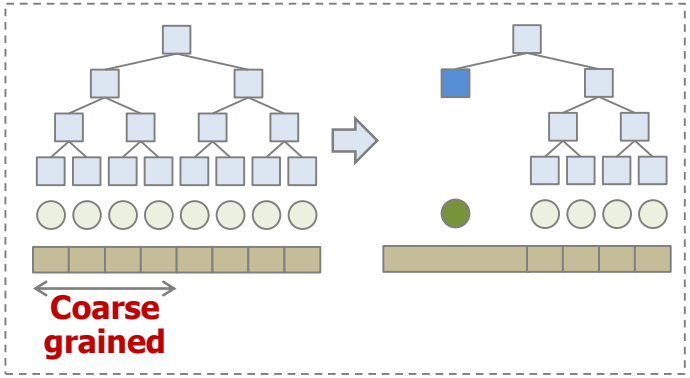
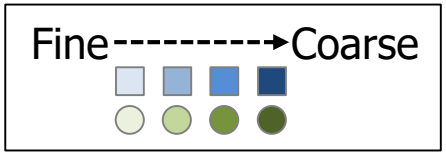
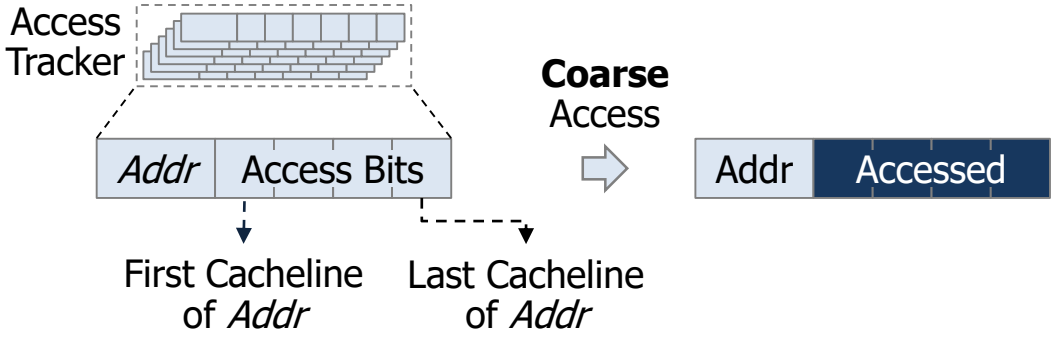
  - Consecutive access bits are set

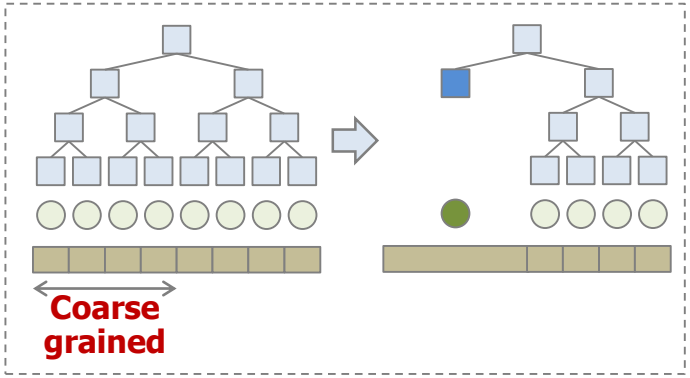


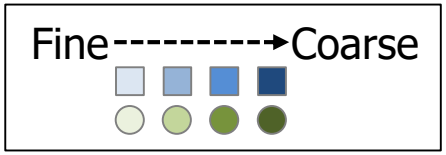



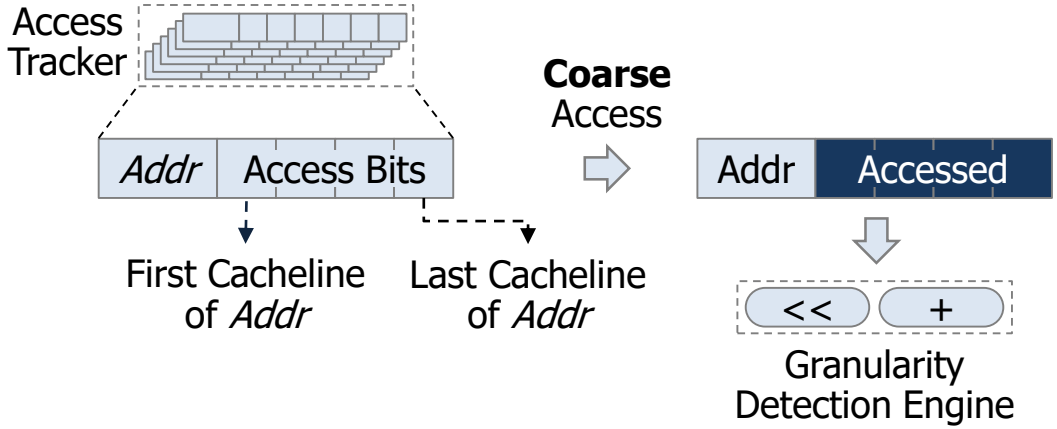



# Granularity Detection (Fine → Coarse)

- Access tracker
  - Records accessed addresses
  - Consecutive access bits are set
- Granularity detection engine
  - Computes a new granularity

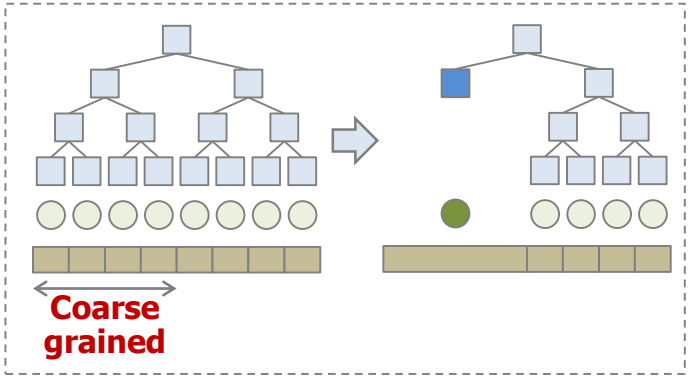


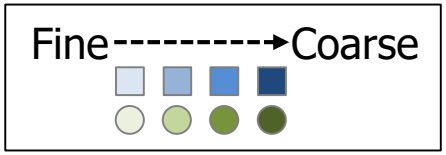



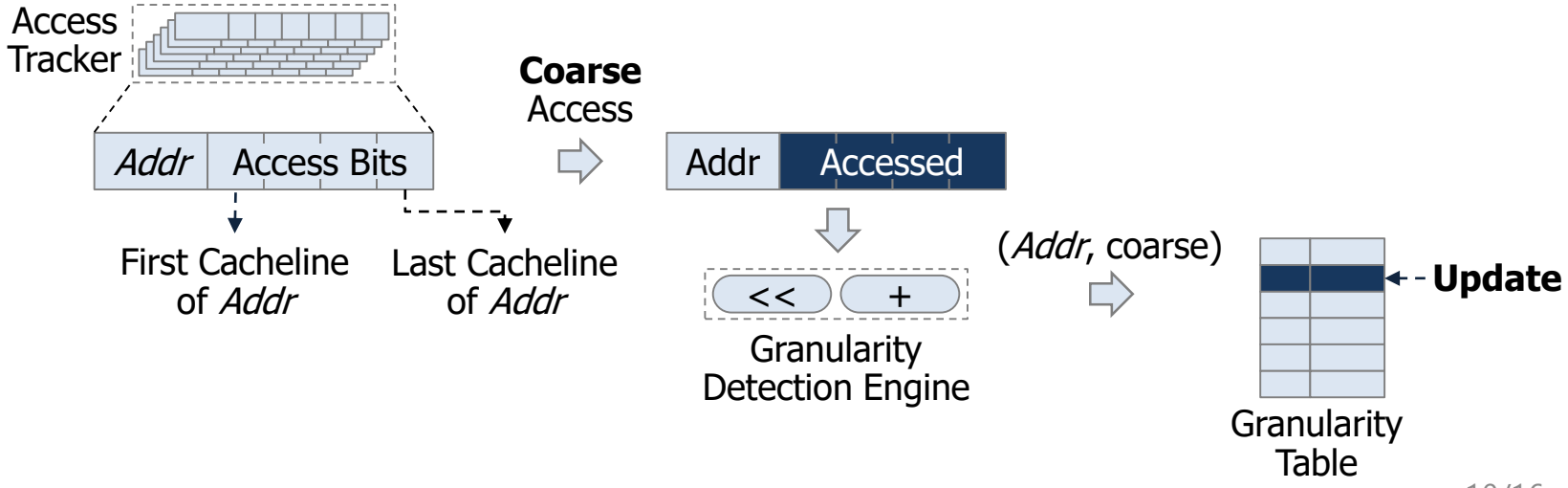



# Granularity Detection (Fine → Coarse)

- Access tracker
  - Records accessed addresses
  - Consecutive access bits are set
- Granularity detection engine
  - Computes a new granularity
  - Updates granularity table

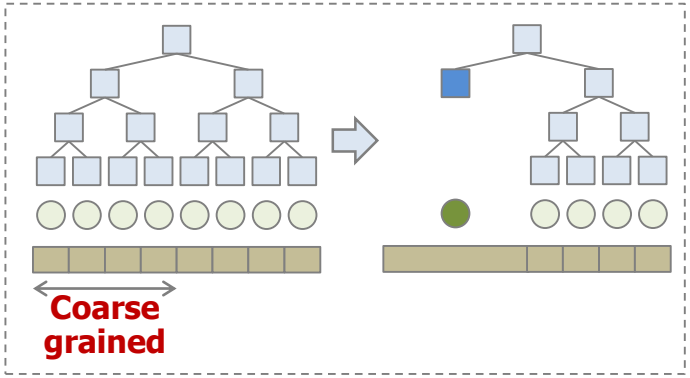


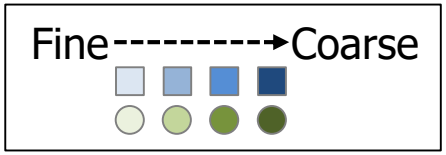



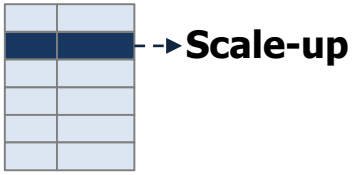



# Granularity Switching (Fine → Coarse)

- Granularity switching engine



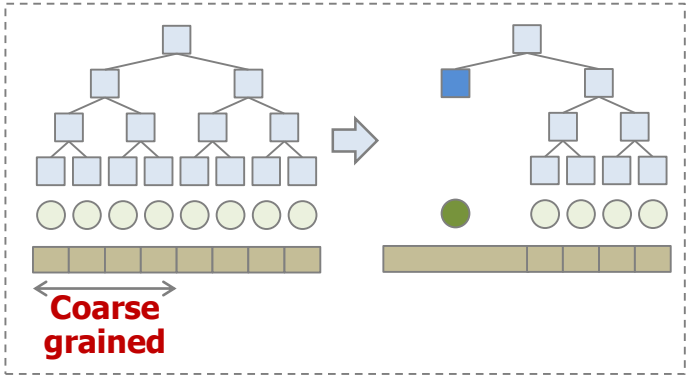



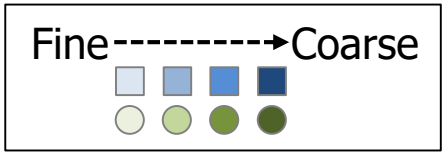

Granularity
Table

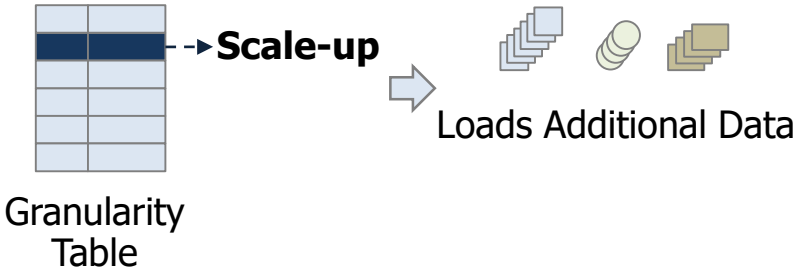
# Granularity Switching (Fine → Coarse)

- Granularity switching engine
  - Loads additional data

    → Old counters, MACs, data blocks



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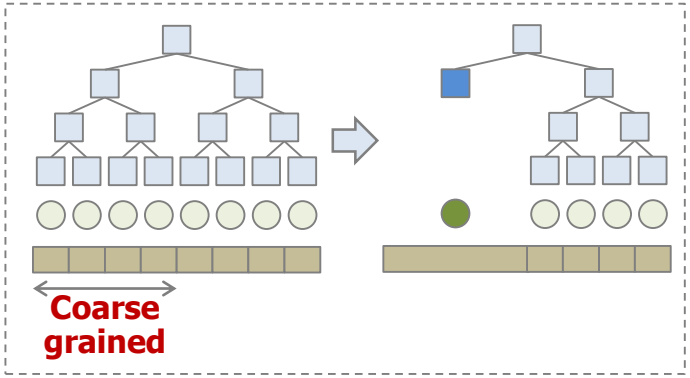


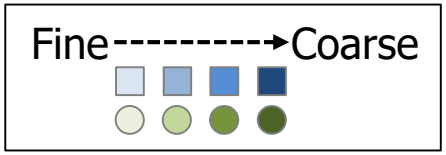


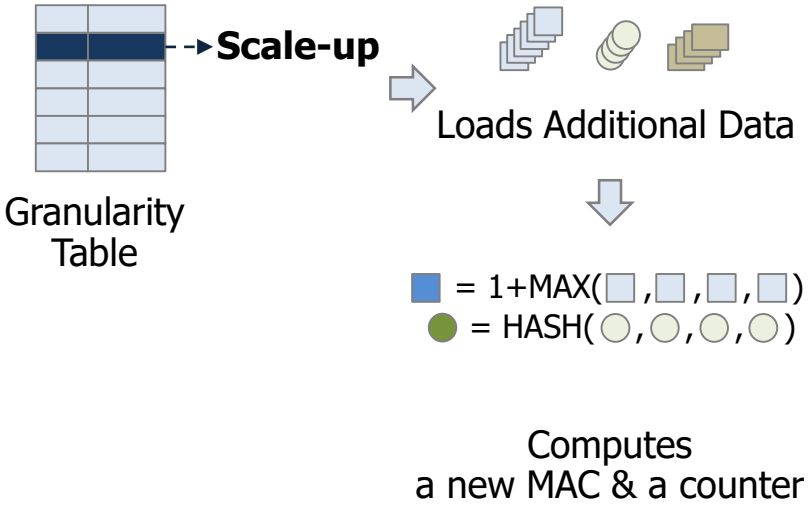

# Granularity Switching (Fine → Coarse)

- Granularity switching engine
  - Loads additional data
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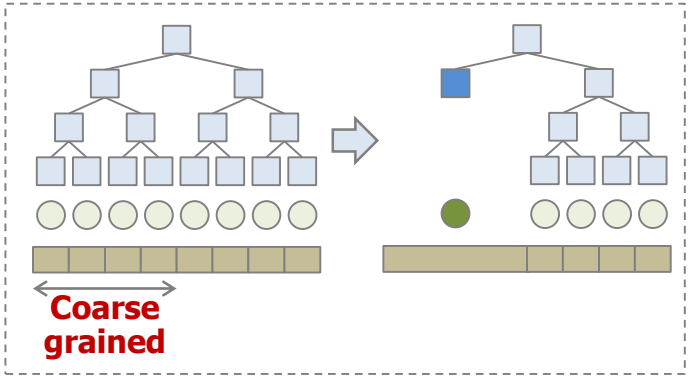
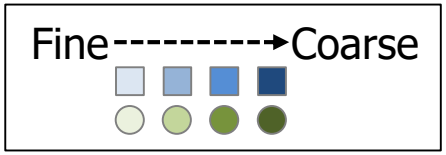
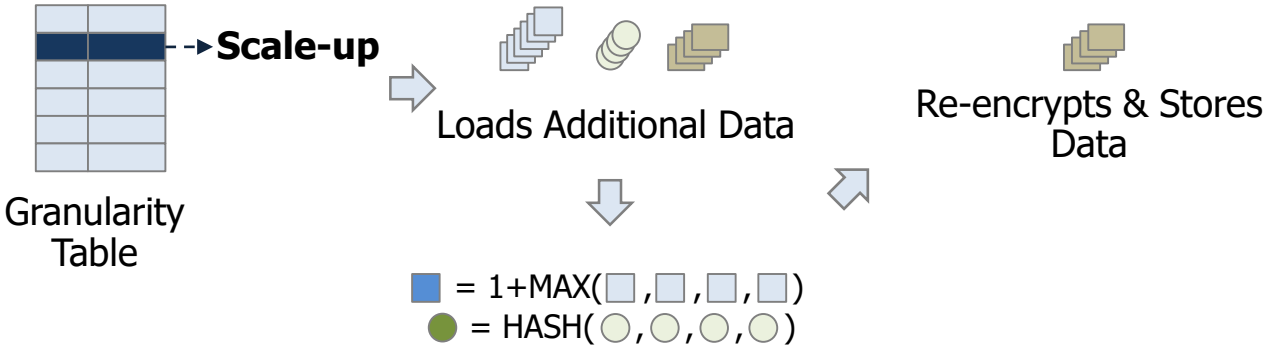
  - Computes counters, MACs
  - Re-encrypts old data



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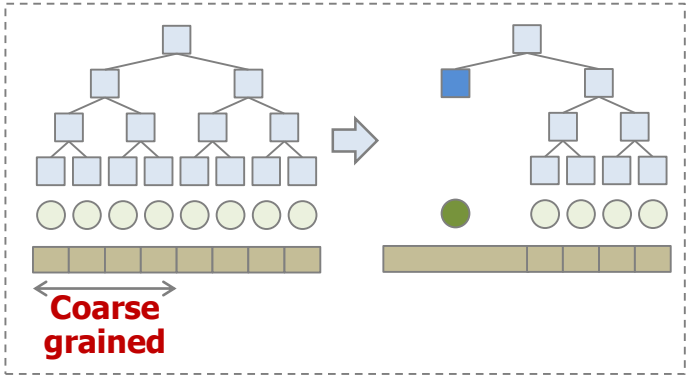
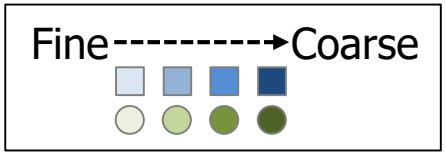
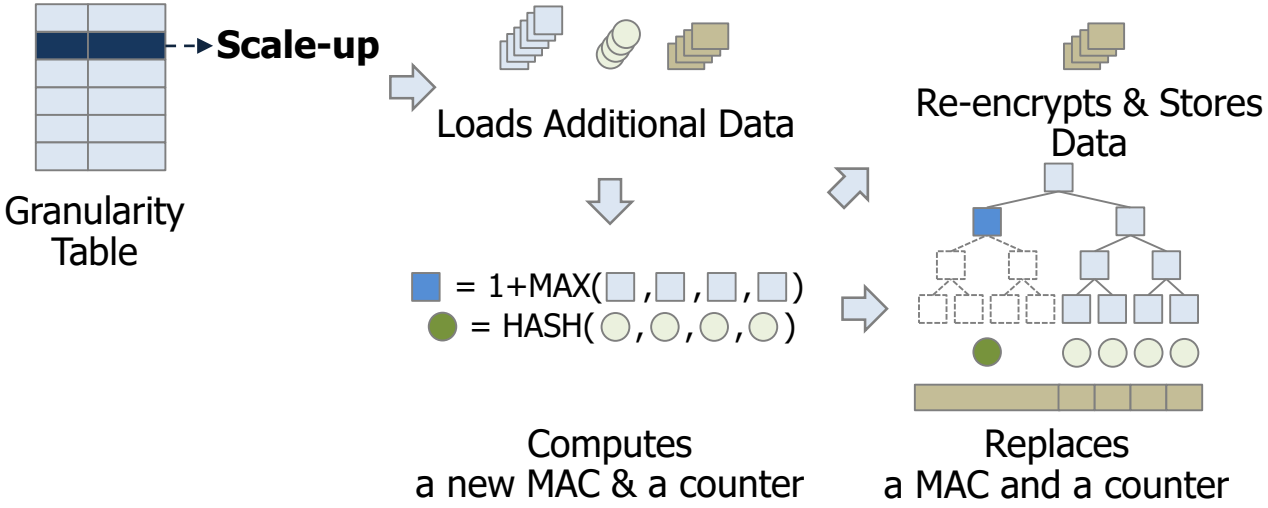
  - Updates & prunes integrity tree



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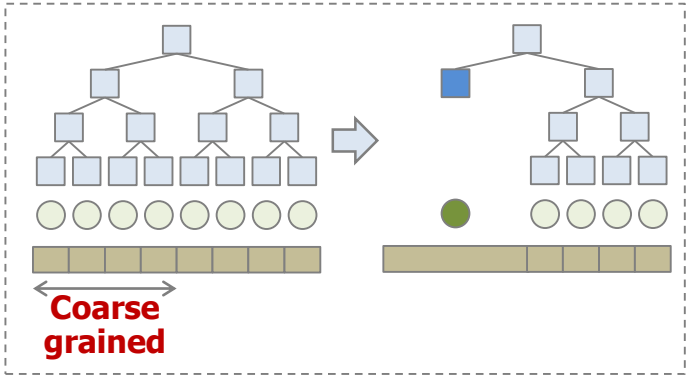


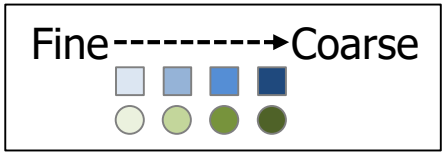


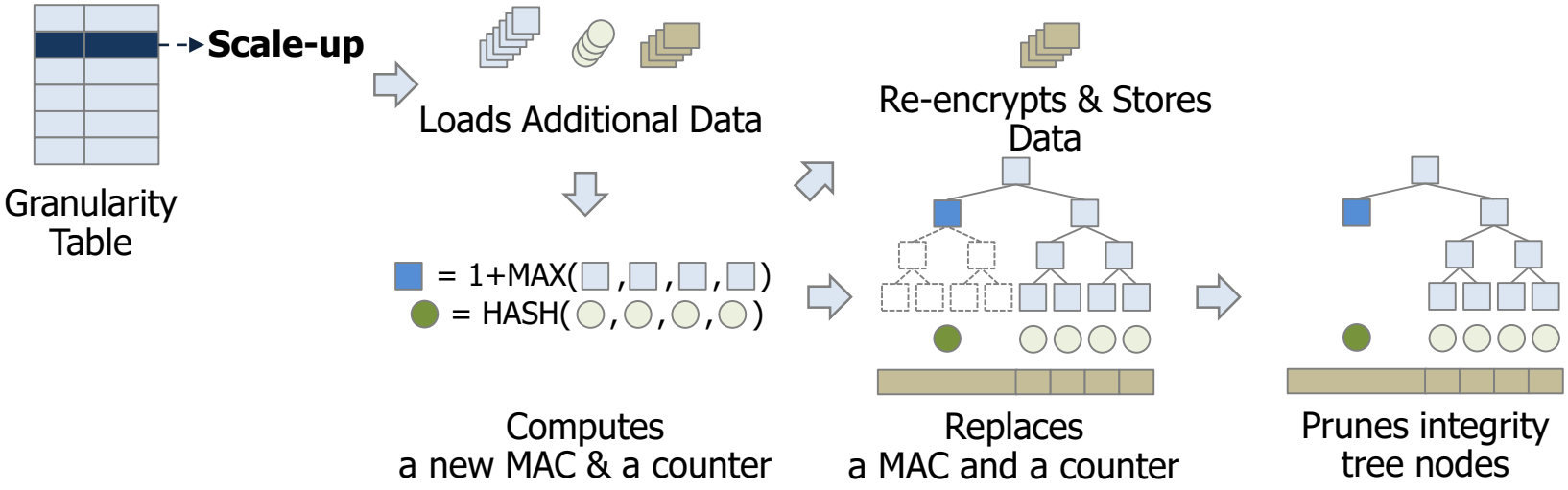

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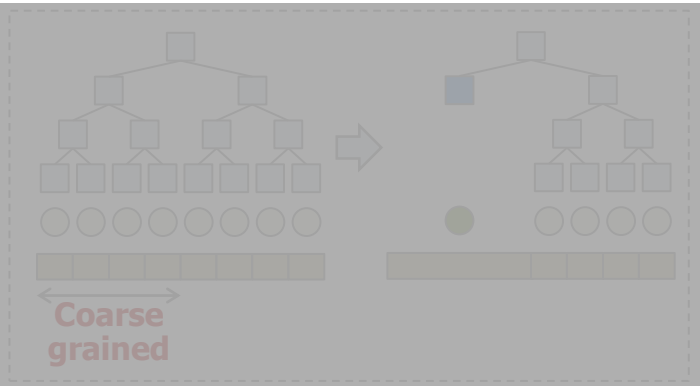
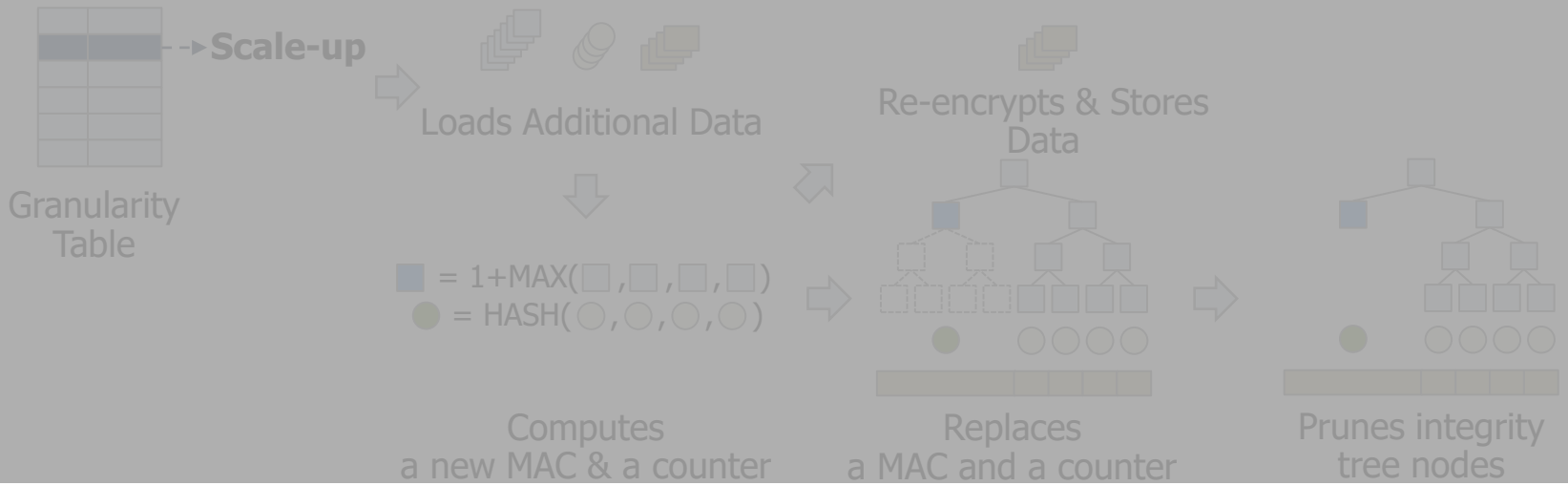



**Granularity switching requires significant overhead → Lazy switching**



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- Configuration: Similar to NVIDIA Orin
  - ARM Cortex CPU + Ampere GPU + 2 x NVDLA with LPDDR4

| | CPU (Jetson AGX Orin ARM Cortex) | GPU (Jetson AGX Orin Ampere) | NPU (NVDLA) |
|---|---|---|---|
| Compute Engine | 8-core | 14 SMs | 45 x 45 Systolic Array |
| On-chip Storage | Cache (L1: 64KB, L2: 2MB) | Cache (L1: 192 KB, L2: 4MB) | Scratchpad Memory (2.2MB in total) |
| Frequency | 2.2GHz | 1GHz | 1GHz |
| Memory System | 2.4GHz, 17GB/s, LPDDR4 Memory System | | |

# Evaluation Environment

- Workloads & Scenarios
  - 14 workloads, 250 scenarios (all combinations)

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  - Access pattern: Fine – ff – f – c – cc – Coarse | Diverse (d)
  - Traffic per cycles: Small (s) – Medium (m) – Large (l)

| | Workloads (access pattern-traffic per cycles) |
|---|---|
| CPU | bw (ff-s), gcc (ff-s), mcf (ff-m), xal (f-m), ray (ff-s) |
| GPU | syr2k (ff-m), pr (f-m), sten (c-l), mm (cc-m), floyd (d-s), |
| NPU | ncf (c-s), dlrm (c-s), sfrnn (c-l), alex (cc-m) |

# Evaluation Result (Avg of Processing Units)

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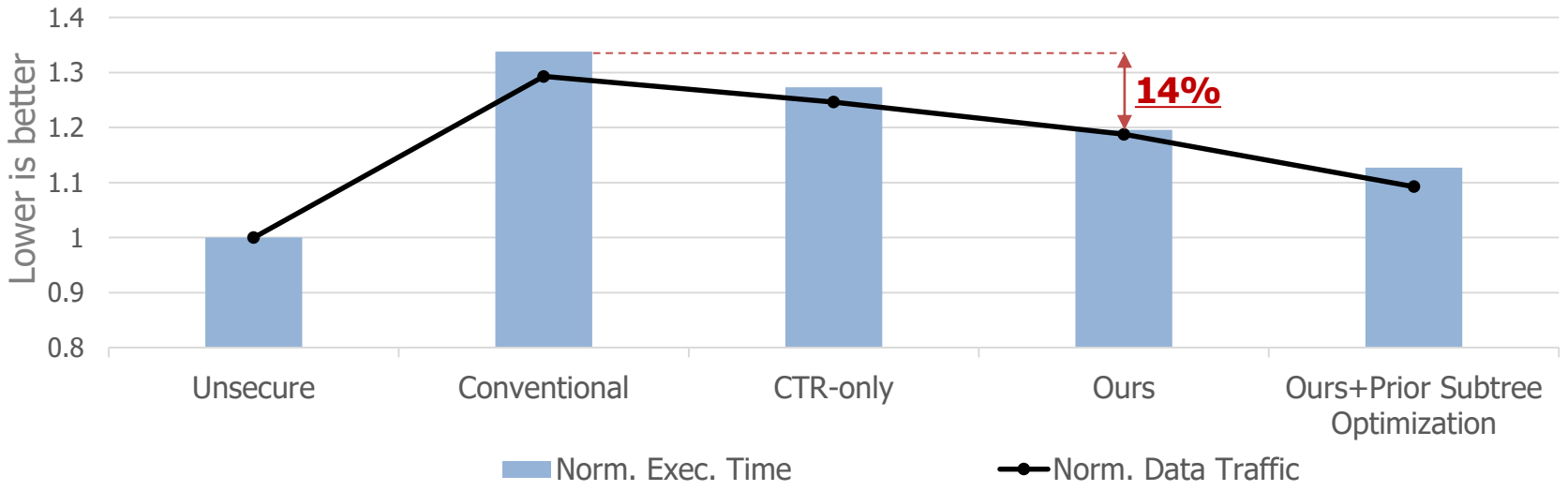
- **14%** improvement with **11%** data reduction



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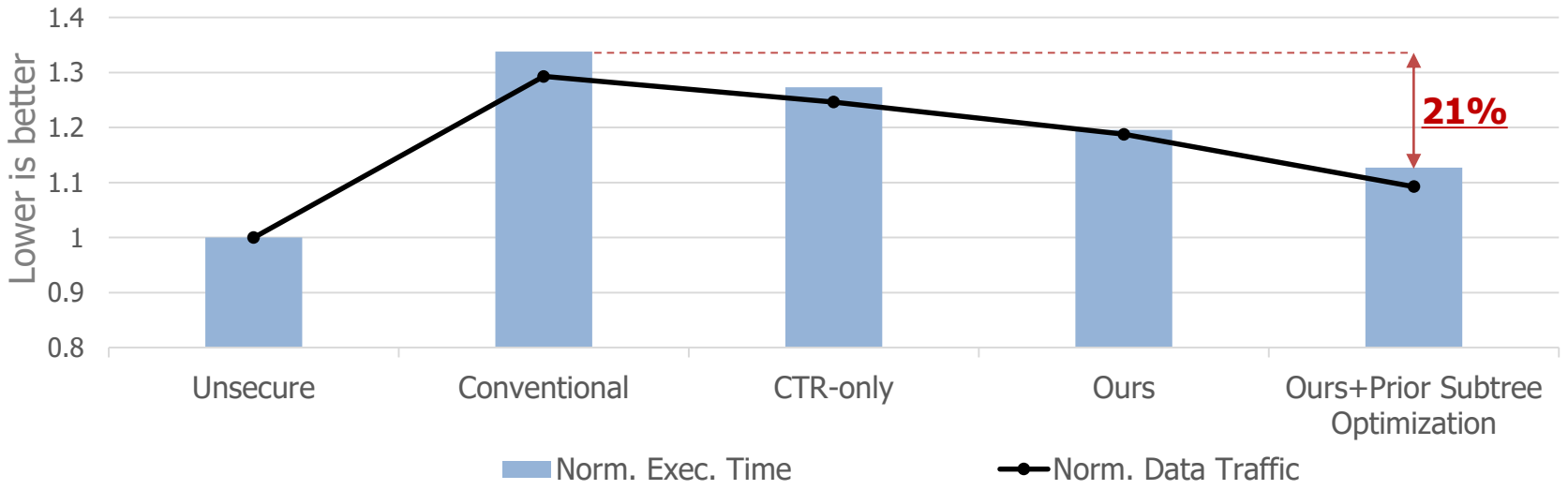
- **14%** improvement with **11%** data reduction
- Combining prior subtree optimization [1-4]
  - Performance improvement: **14%** → **21%**





[1] Bonsai Merkle Forests: Efficiently Achieving Crash Consistency in Secure Persistent Memory (MICRO 2021)
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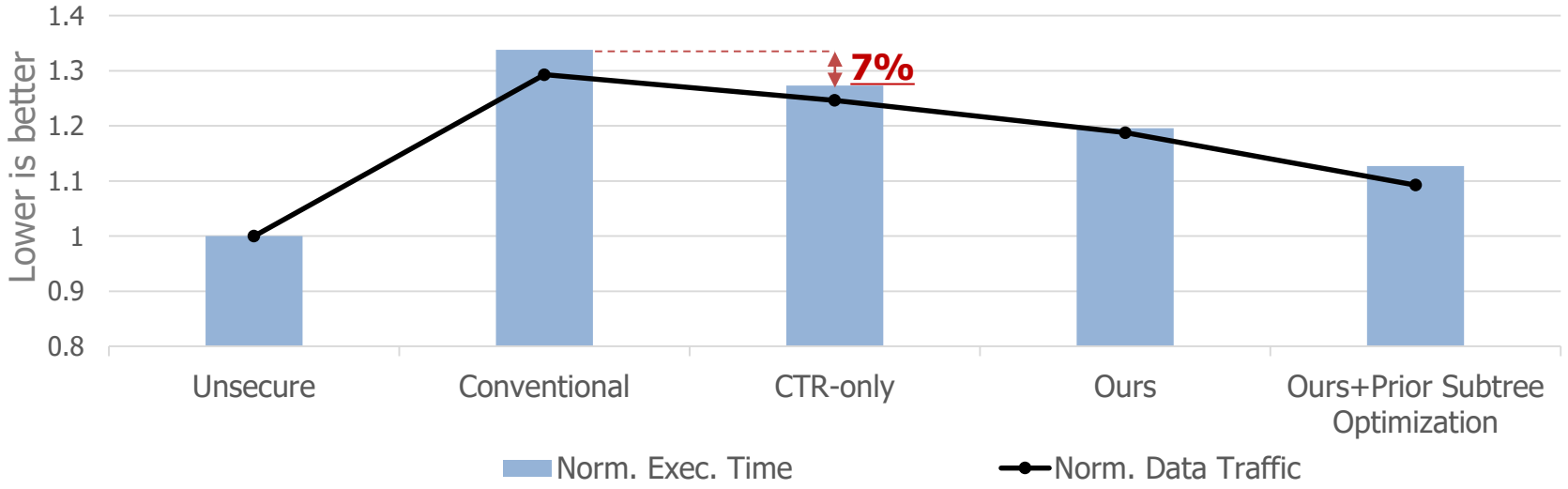



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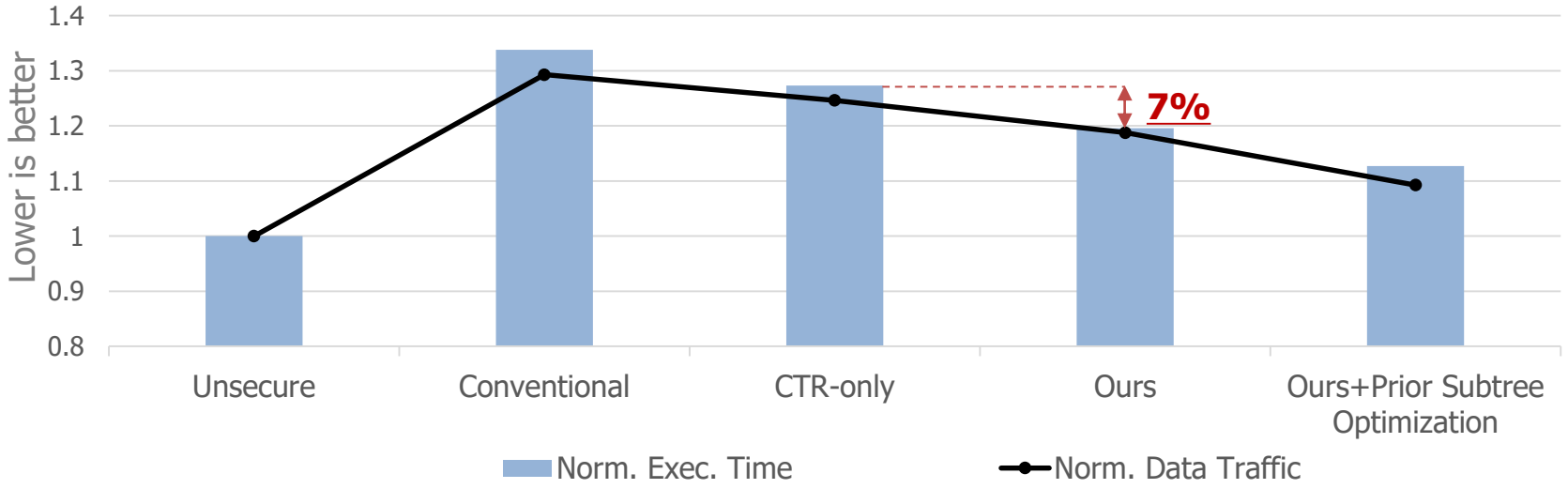



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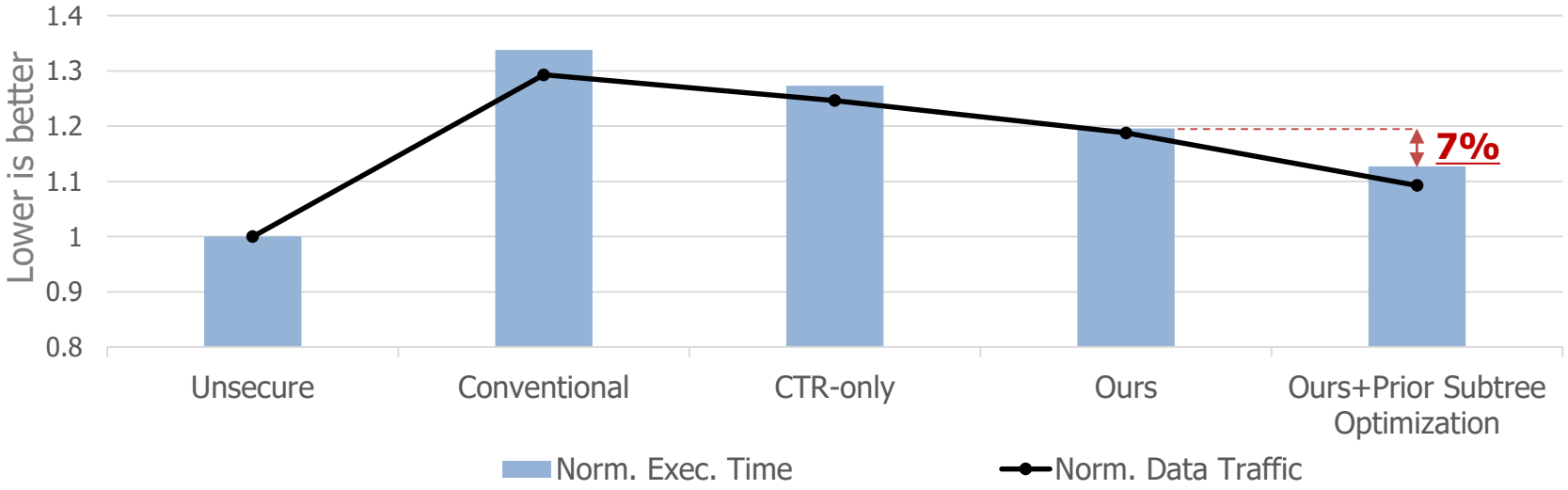



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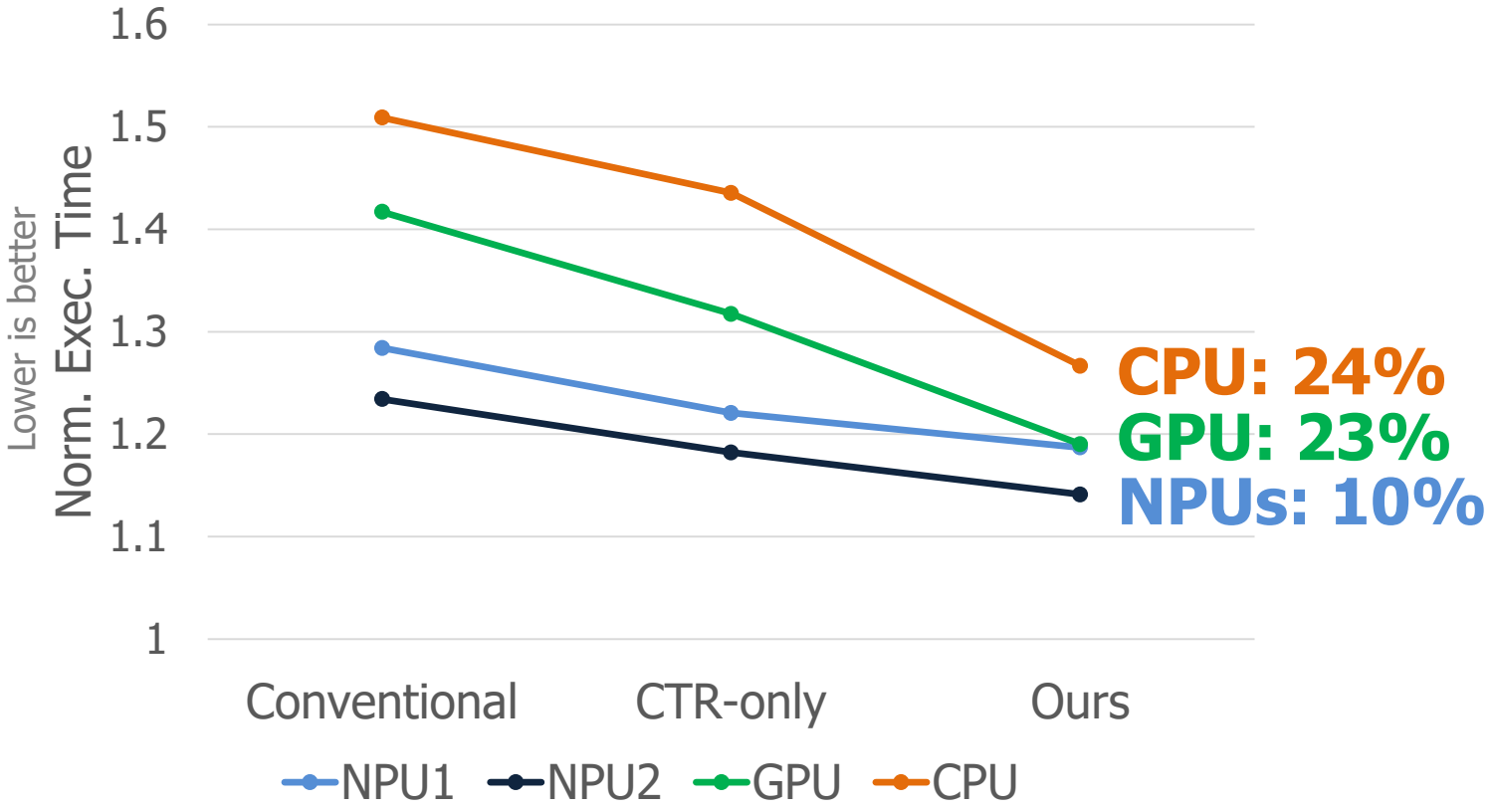
- Performance improvement of each processing unit
  - CPU (**24%**), GPU (**23%**), NPU (**10%**)



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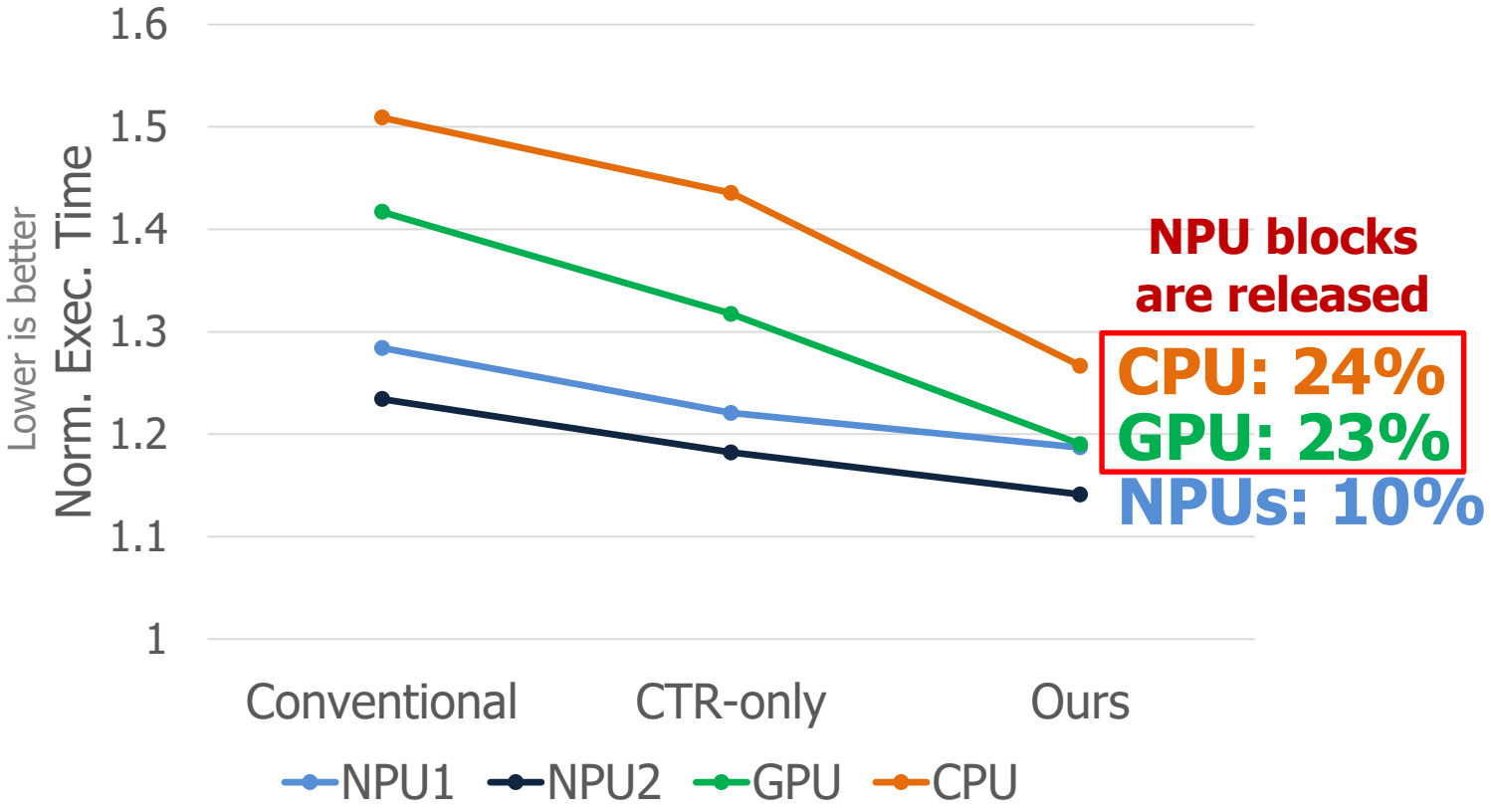

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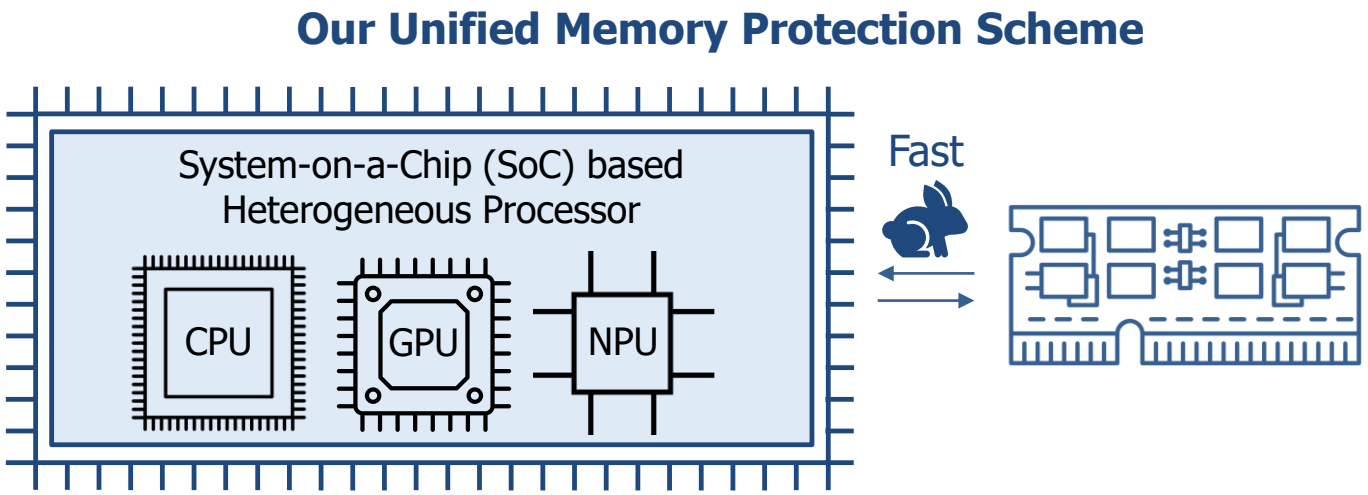
- Unified memory protection for heterogeneous processor



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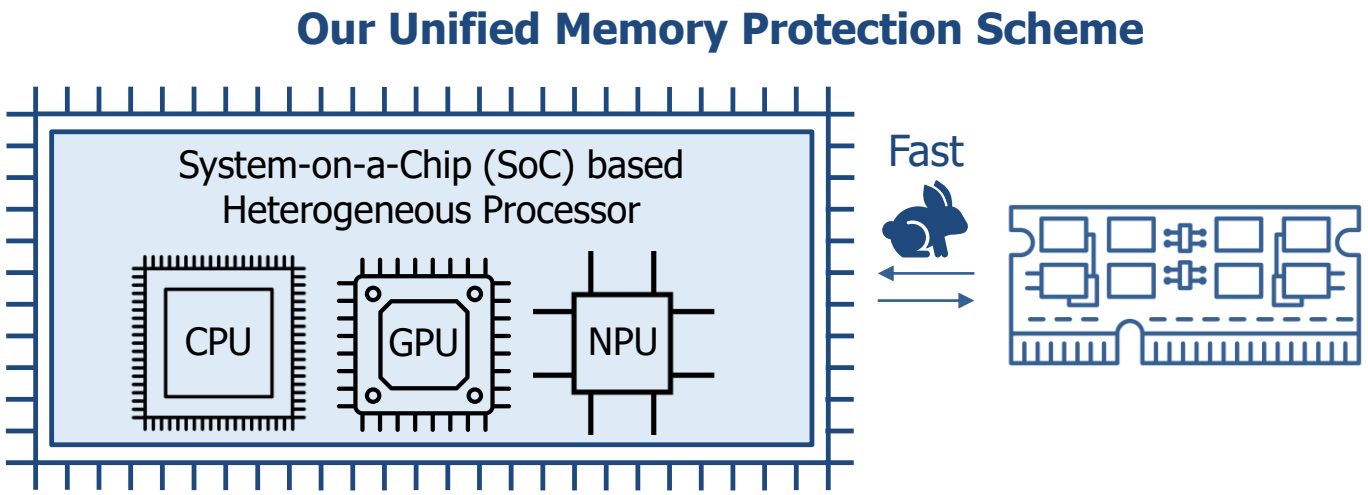

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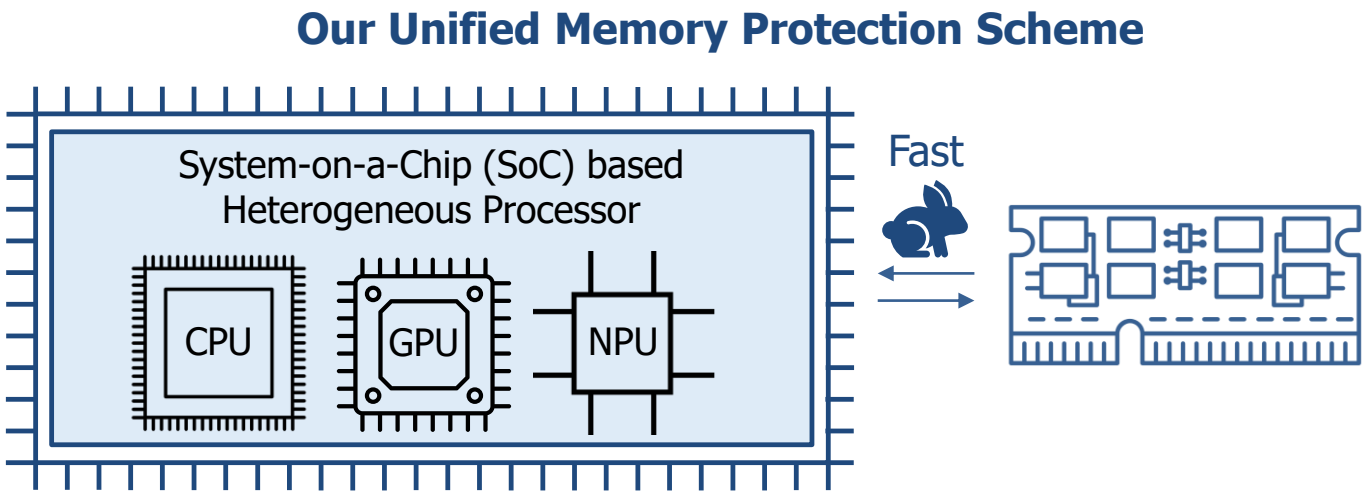
  - Challenge: Diverse access pattern

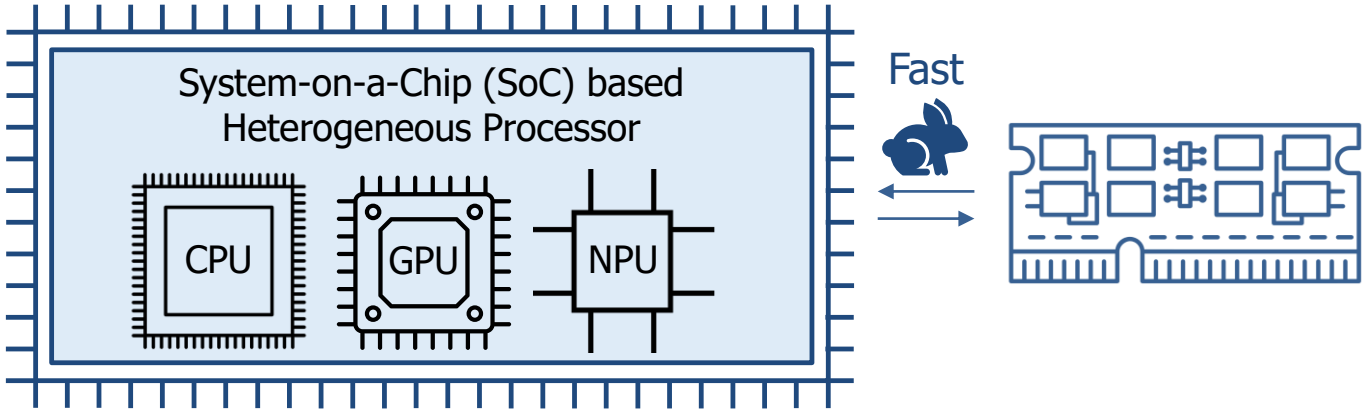


# Conclusion

- Unified memory protection for heterogeneous processor
  - **Multi-granular MAC & Integrity Tree**
  - Challenge: Diverse access pattern

- Improvement: **14%** (w/o subtree opt.), **21%** (w/ subtree opt.)

**Our Unified Memory Protection Scheme**



# Thank you

# Backup Slide

# Detailed Granularity Switching

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* Scale-up (Fine → Coarse)

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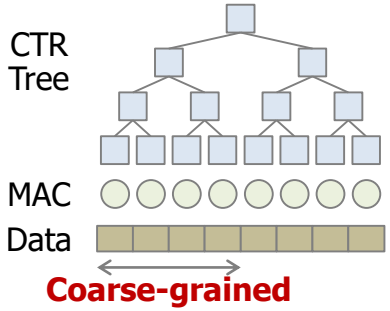
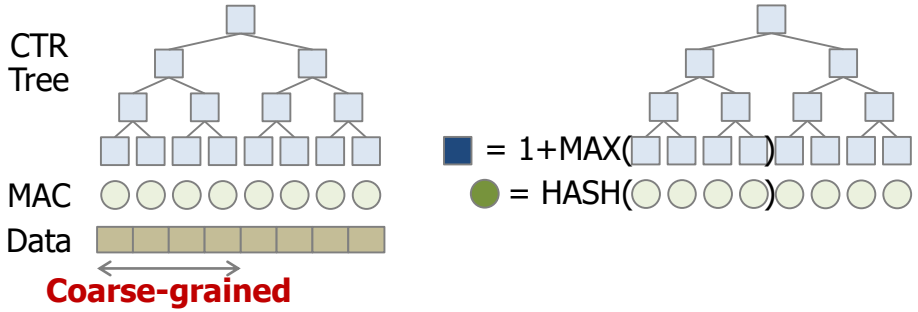



1) Detect scale-up

# Detailed Granularity Switching

* Scale-up (Fine → Coarse)




1) Detect scale-up

2) Compute new MAC/CTR

# Detailed Granularity Switching

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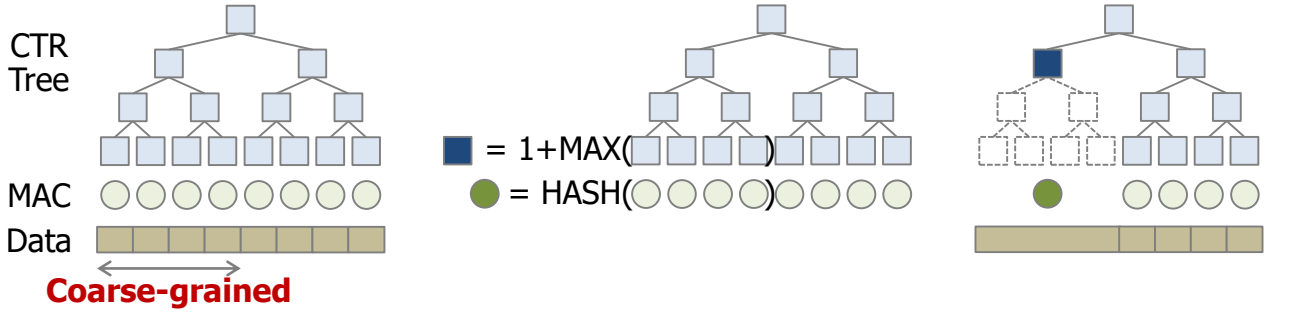


1) Detect scale-up  2) Compute new MAC/CTR  3) Replace MAC/CTR

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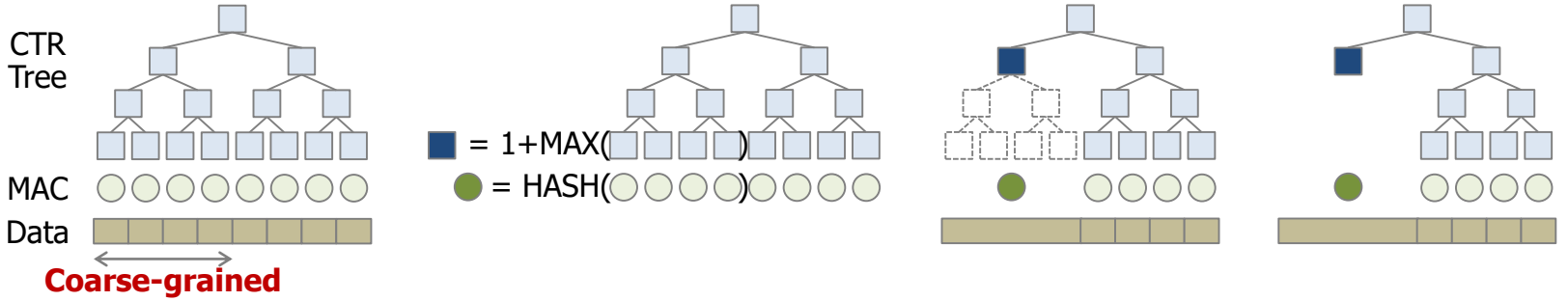


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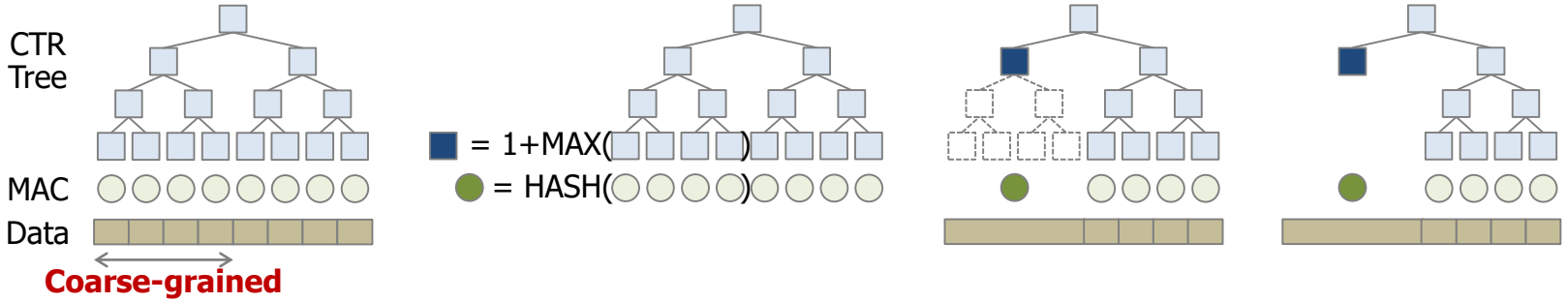


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* Scale-down (Coarse → Fine)

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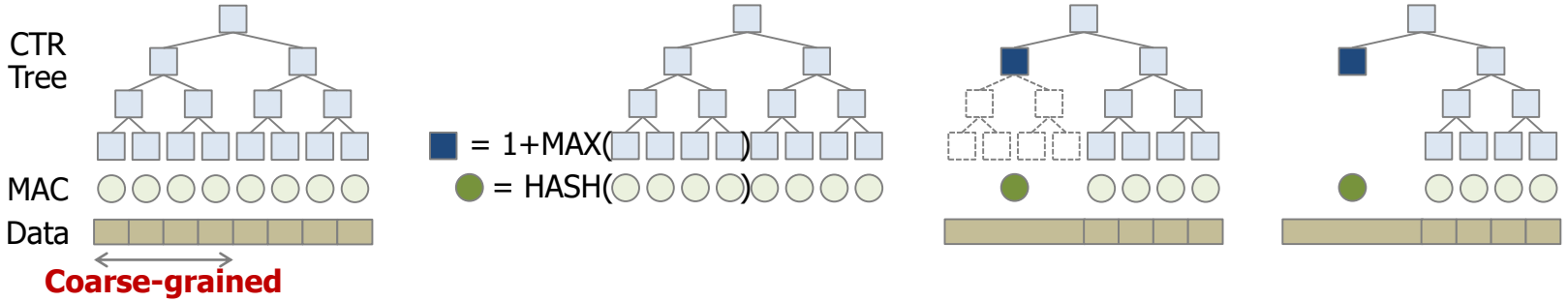


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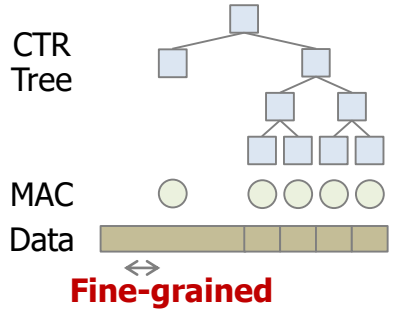
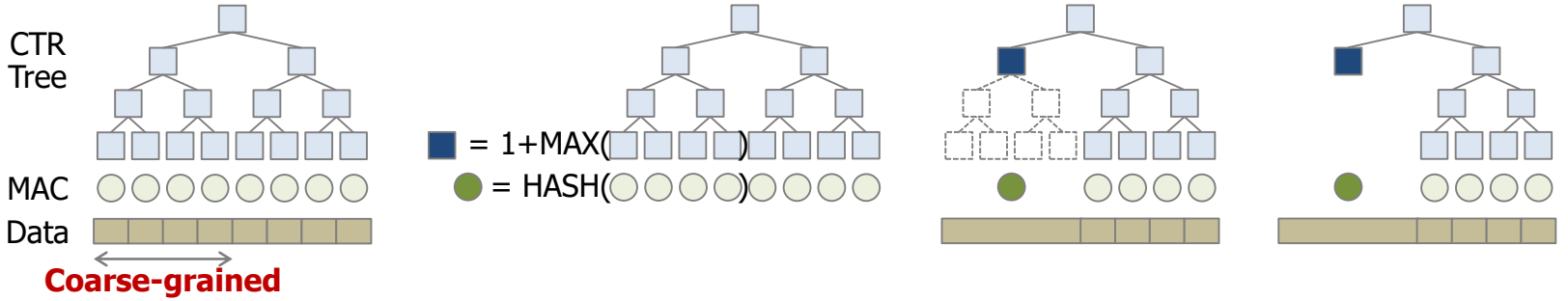



1) Detect scale-down

# Detailed Granularity Switching

* Scale-up (Fine → Coarse)




1) Detect scale-up 2) Compute new MAC/CTR 3) Replace MAC/CTR 4) Prune CTR tree

* Scale-down (Coarse → Fine)


1) Detect scale-down 2) Compute new MAC/CTR

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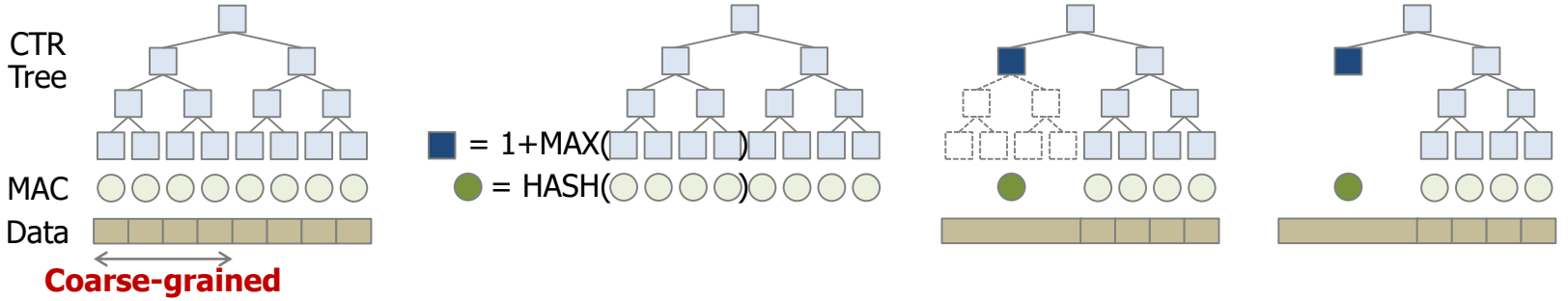


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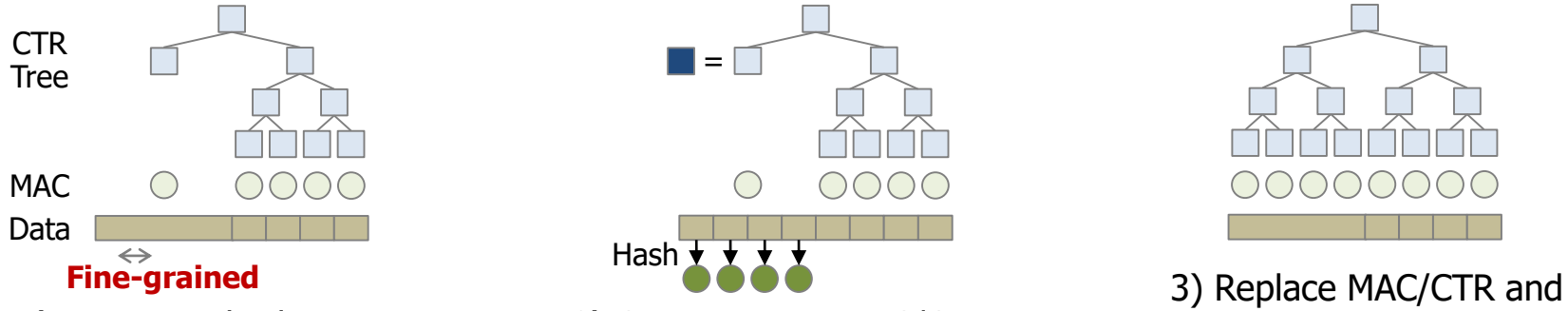


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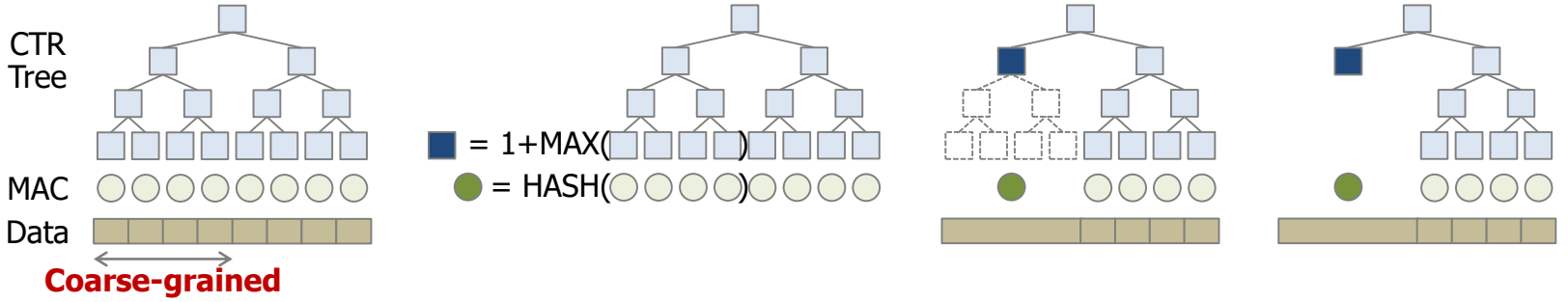


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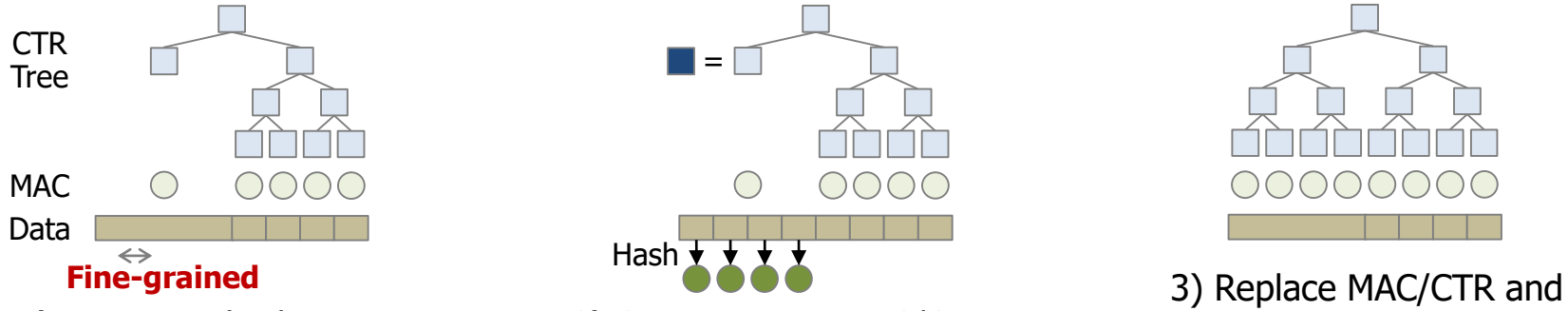


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**Granularity switching requires significant overhead! → Lazy switching**

# Lazy Switching Overhead by MAC

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$$Coarse\ MAC = HASH\ (Fine\ MACs)$$

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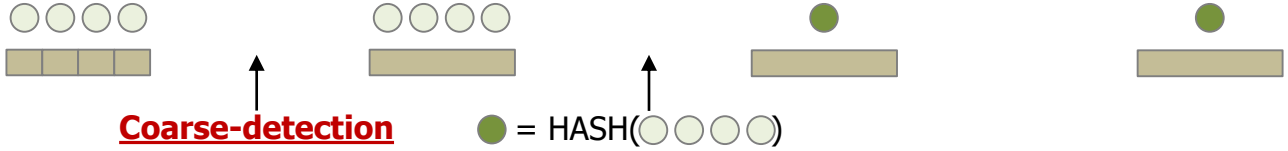

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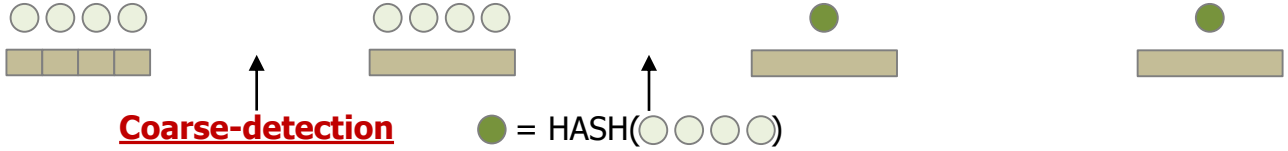


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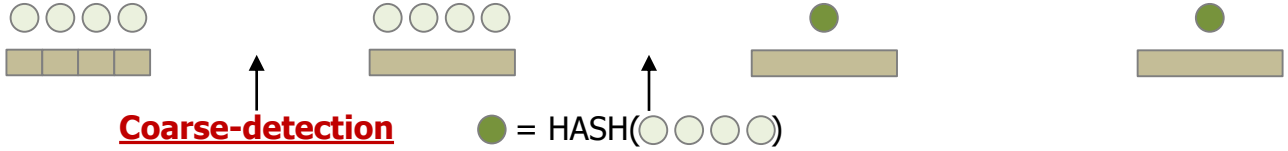


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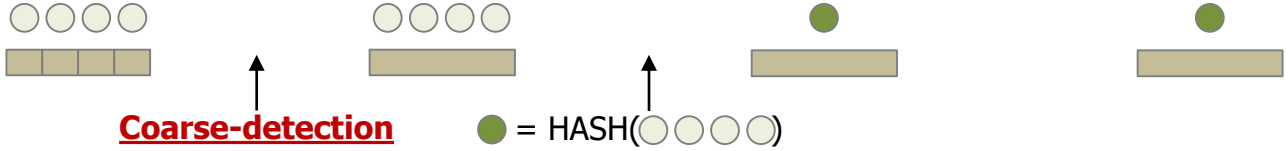


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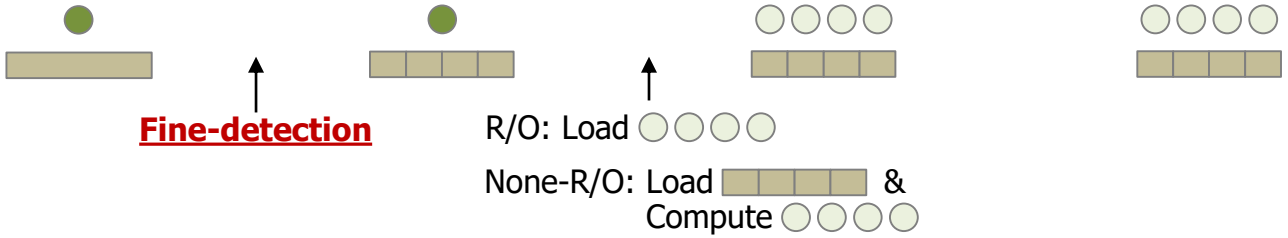

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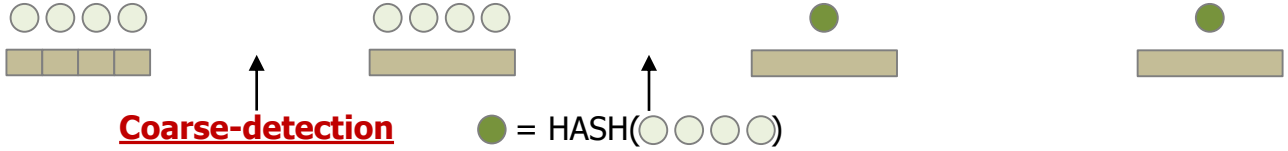


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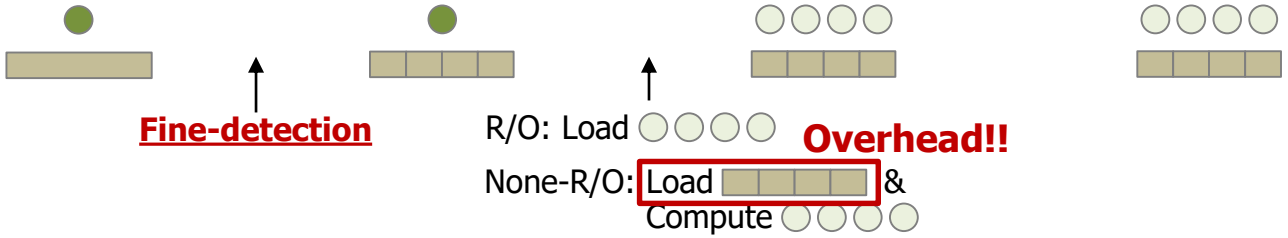

# Lazy Switching Overhead by MAC

- **97.2%** of reqs → Hidden by **lazy switching & R/O**
  - Only **2.8%** of reqs makes moderate overhead (ld data chunks)

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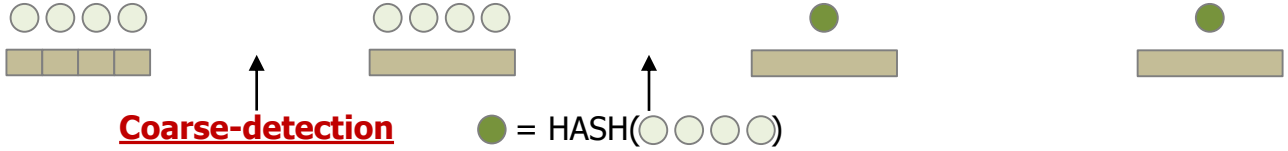


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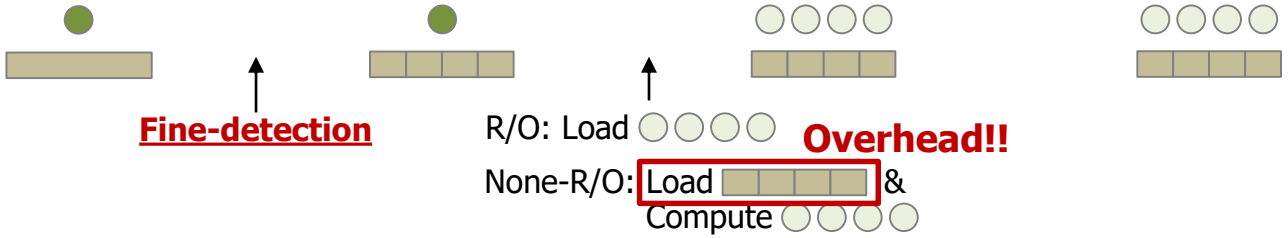

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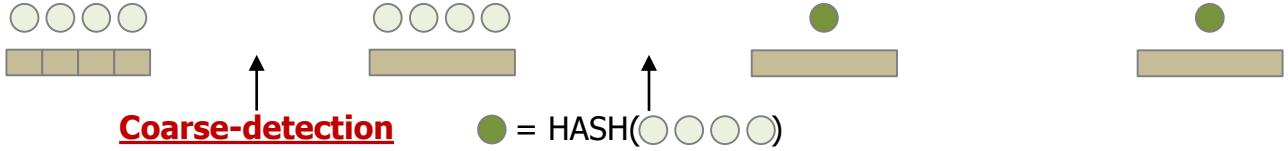


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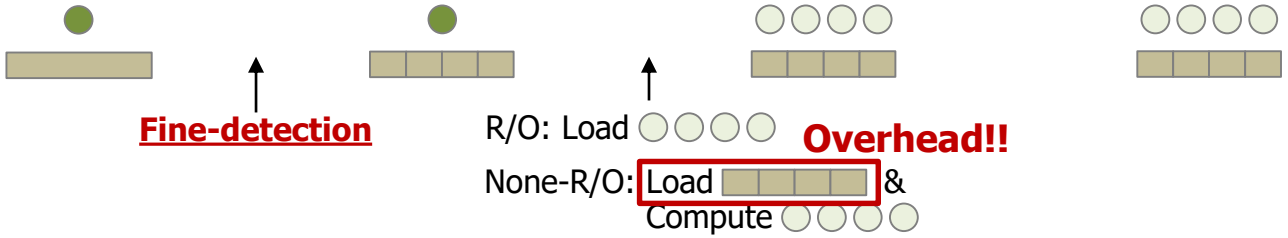


**Lazy switching considerably reduces switching overhead!!**

# Lazy Switching Overhead by CTR Tree

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Granul.
detection

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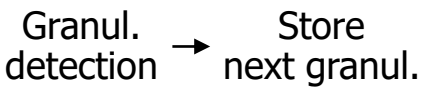

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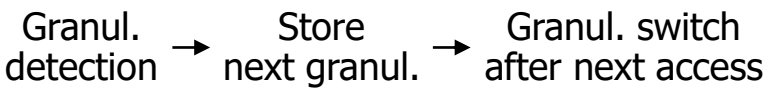

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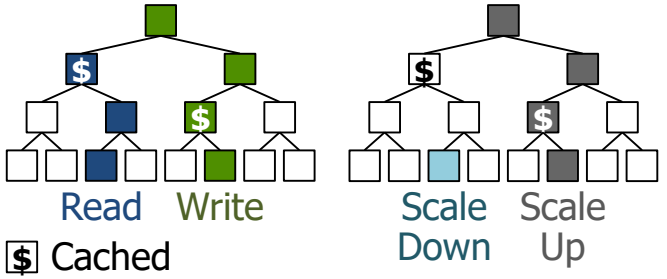

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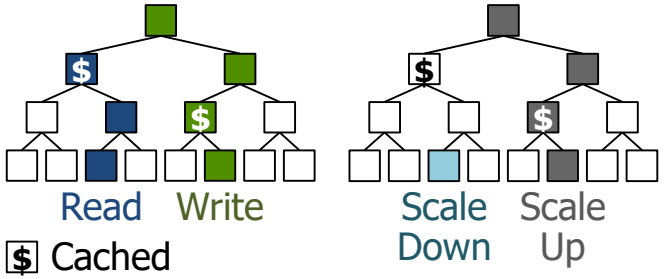


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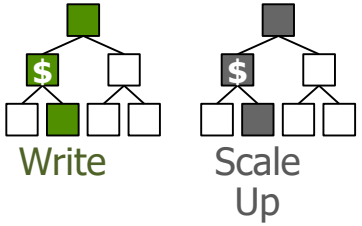

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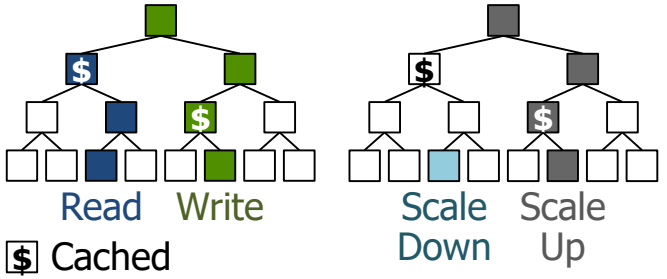


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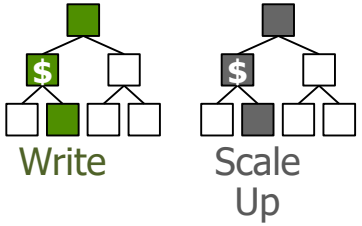


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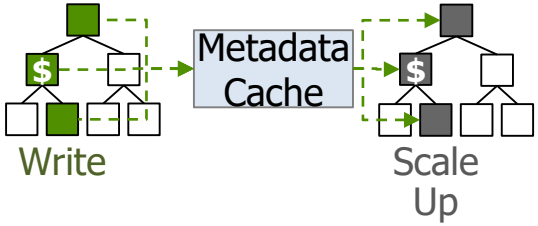

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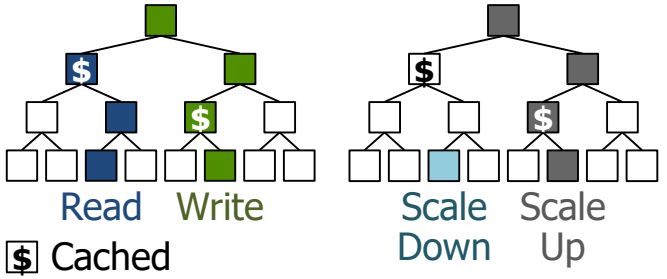


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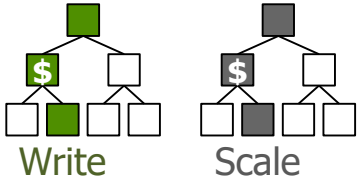


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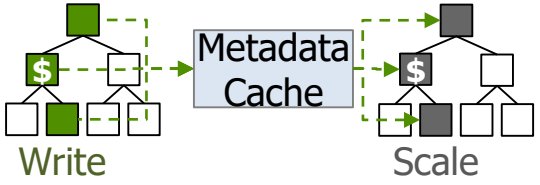


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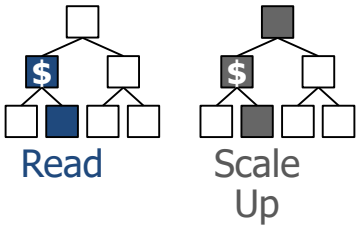

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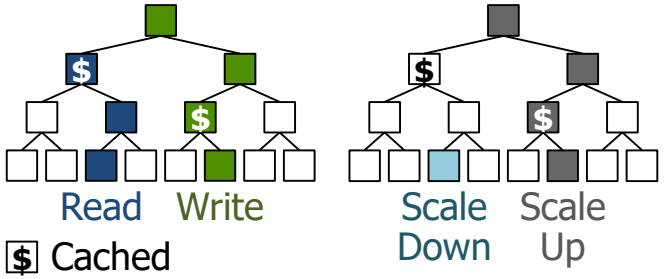


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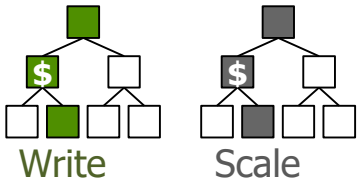


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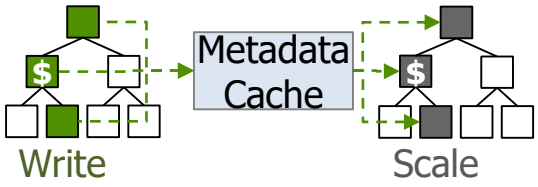


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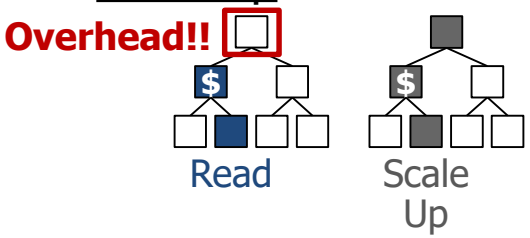

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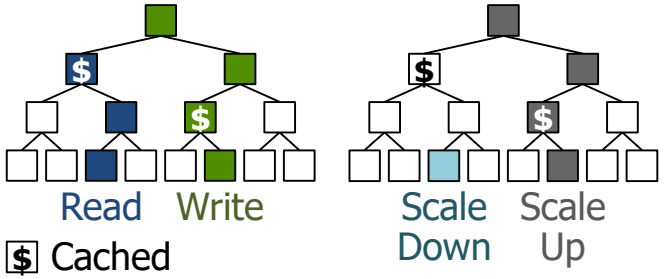


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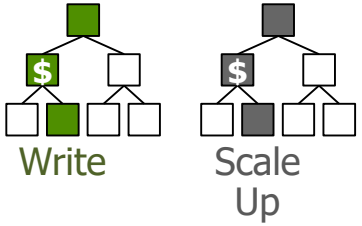


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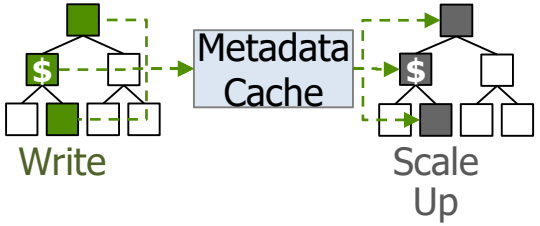


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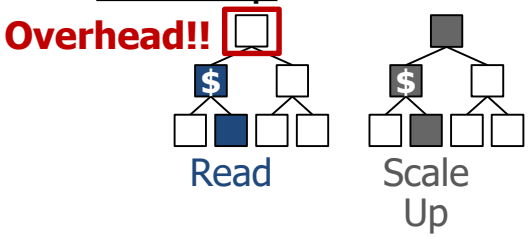


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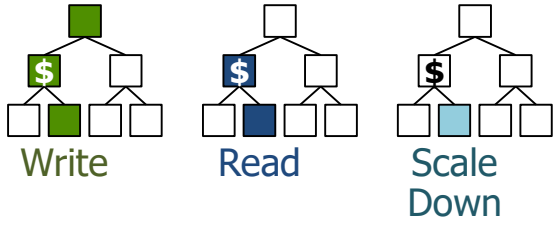


Backup

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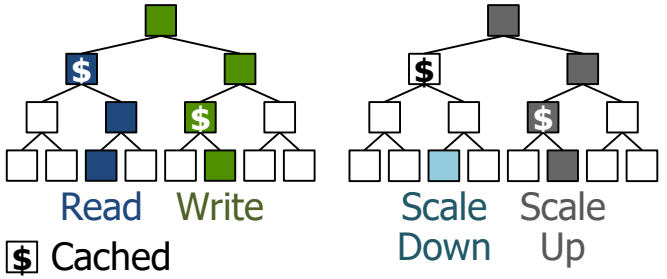


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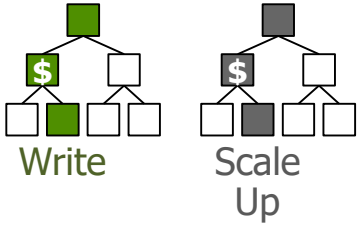


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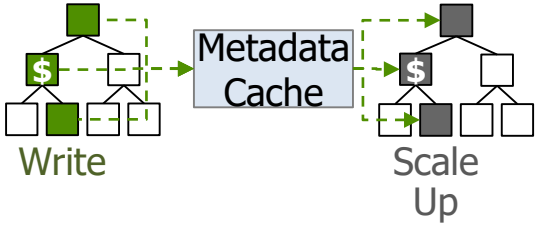


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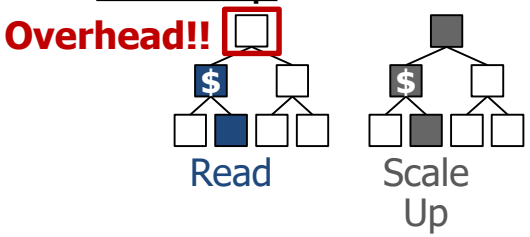


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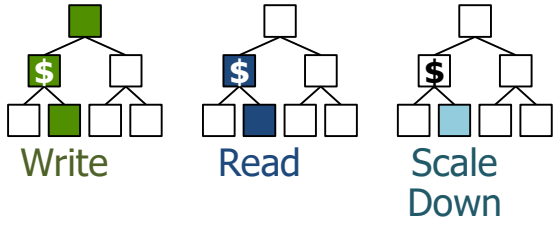


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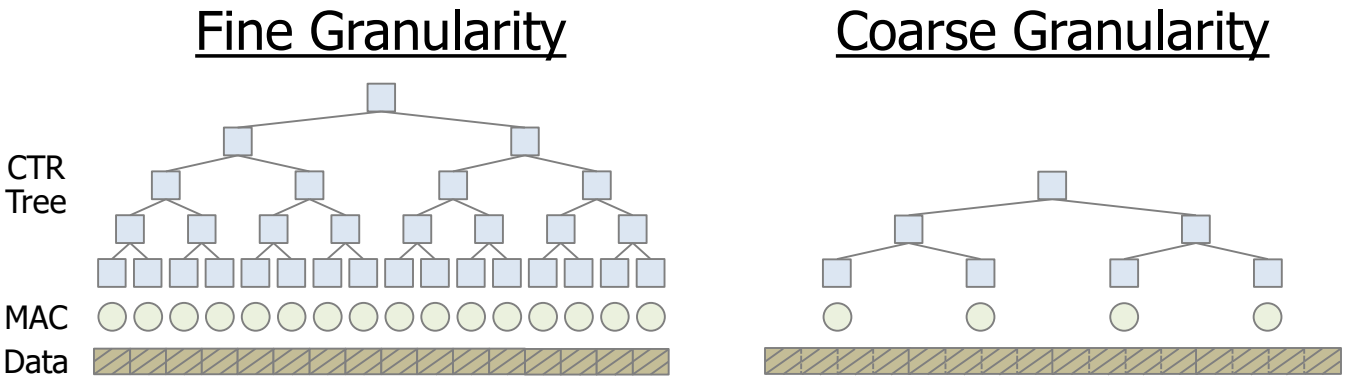

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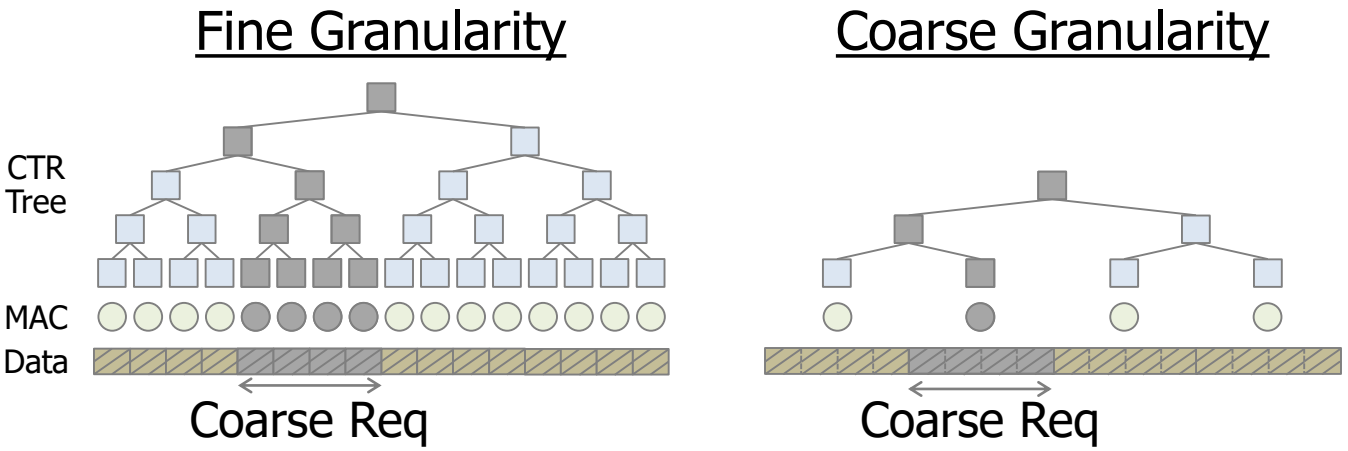


Coarse Reqs

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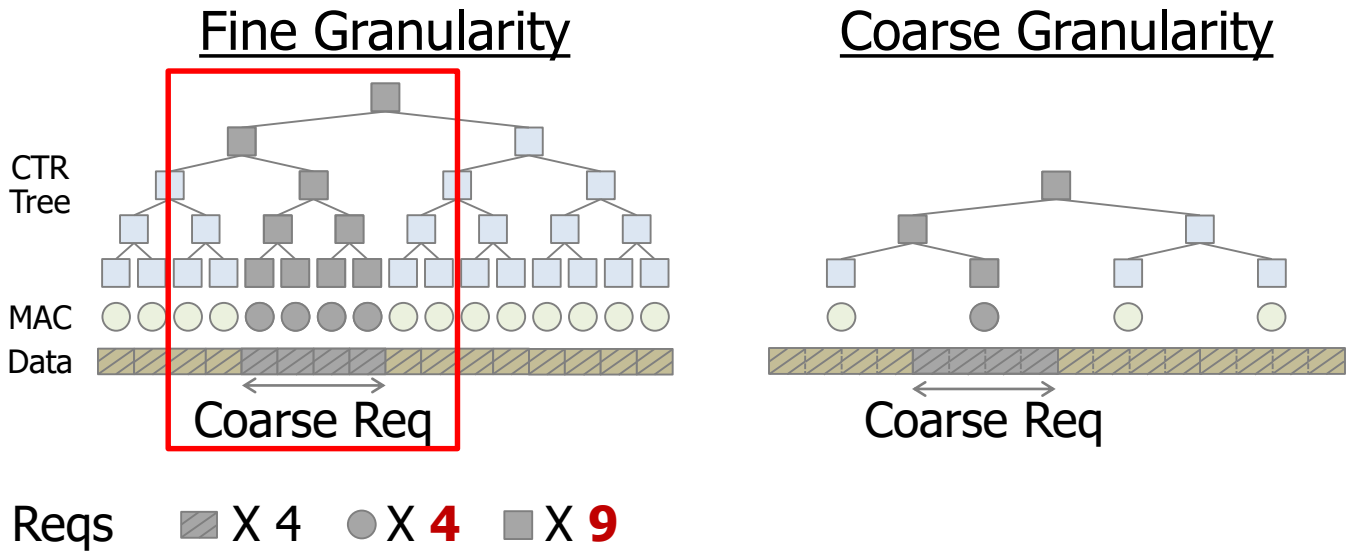

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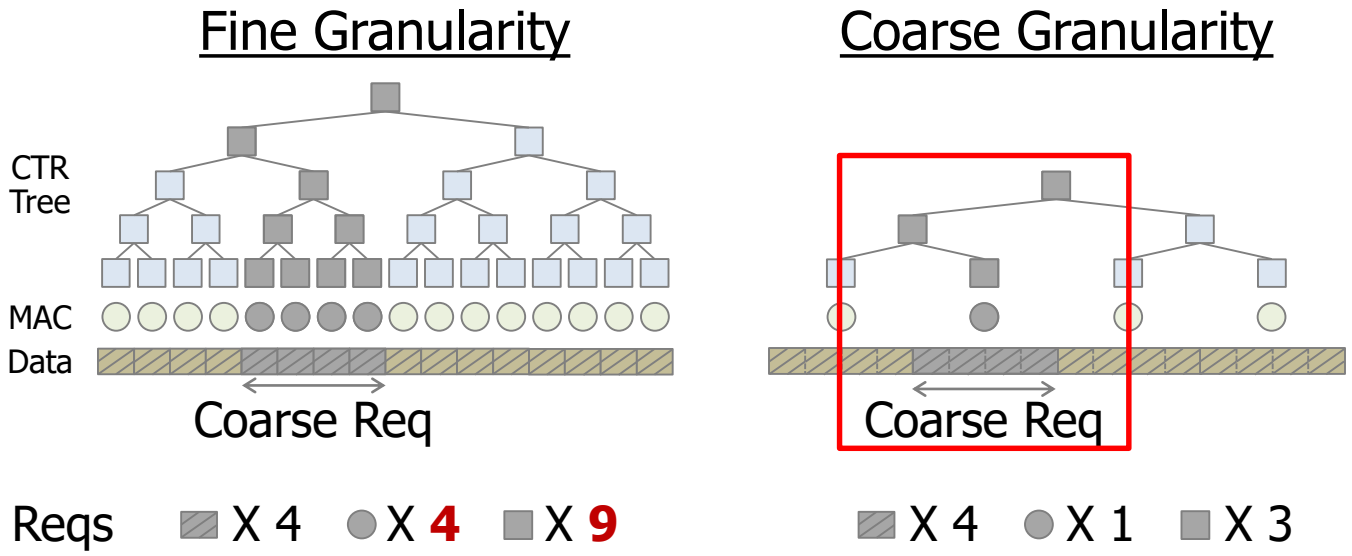

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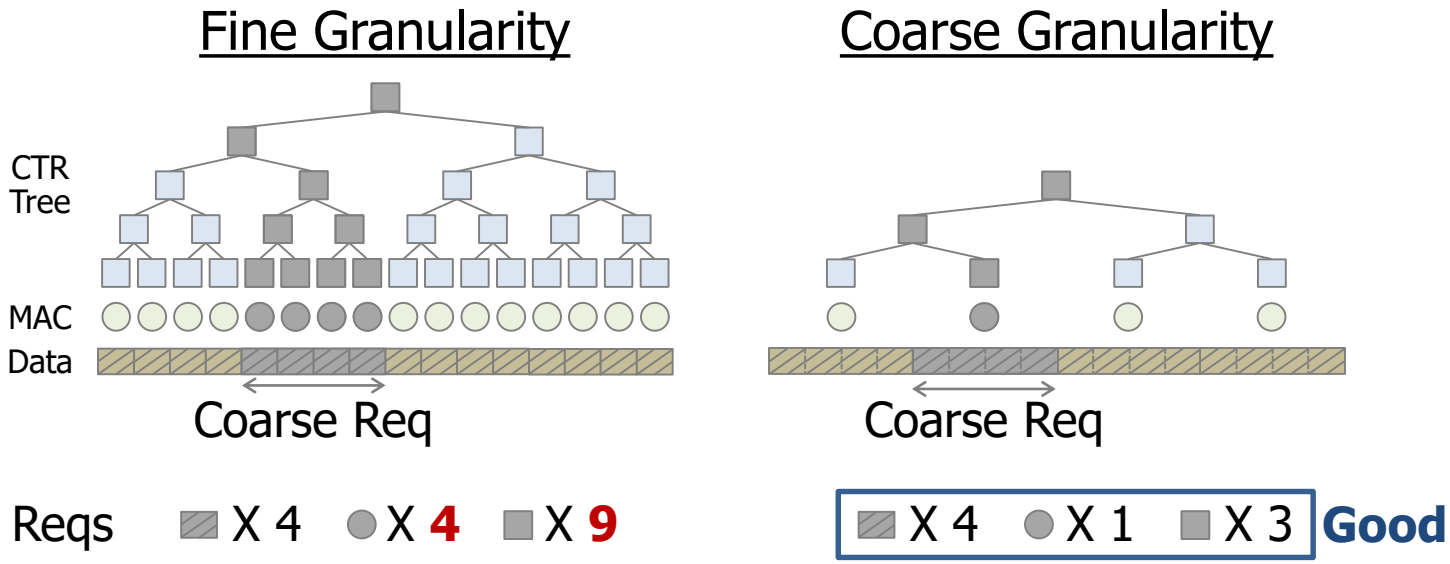

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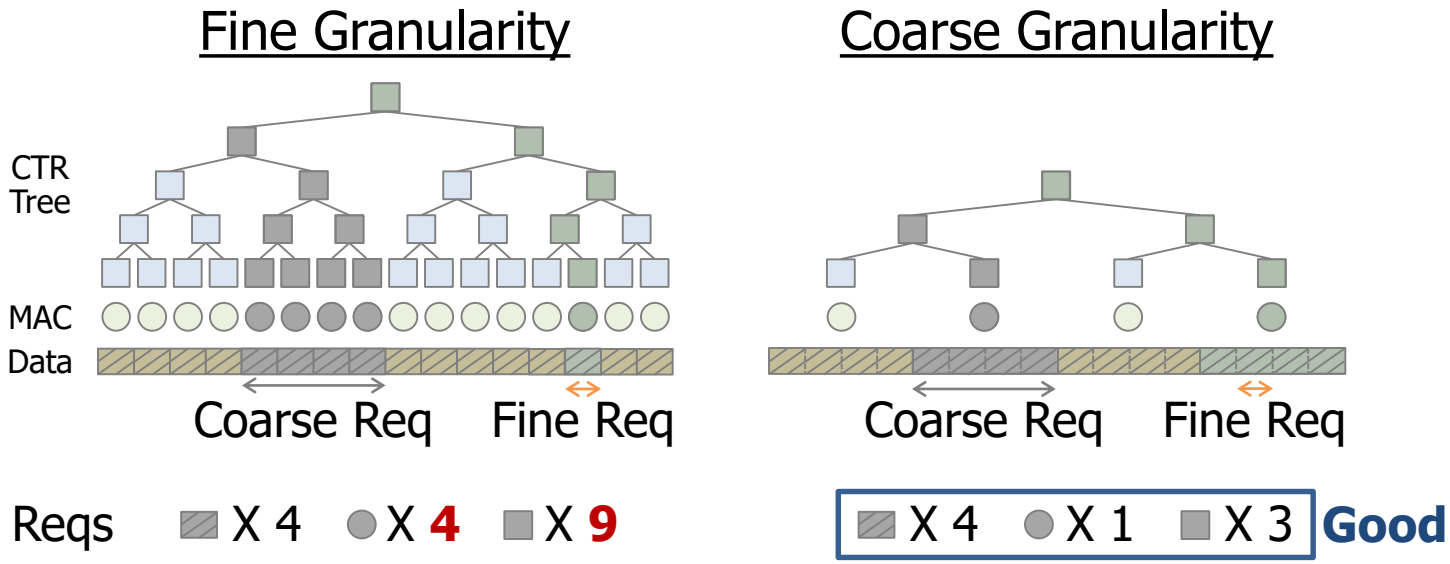

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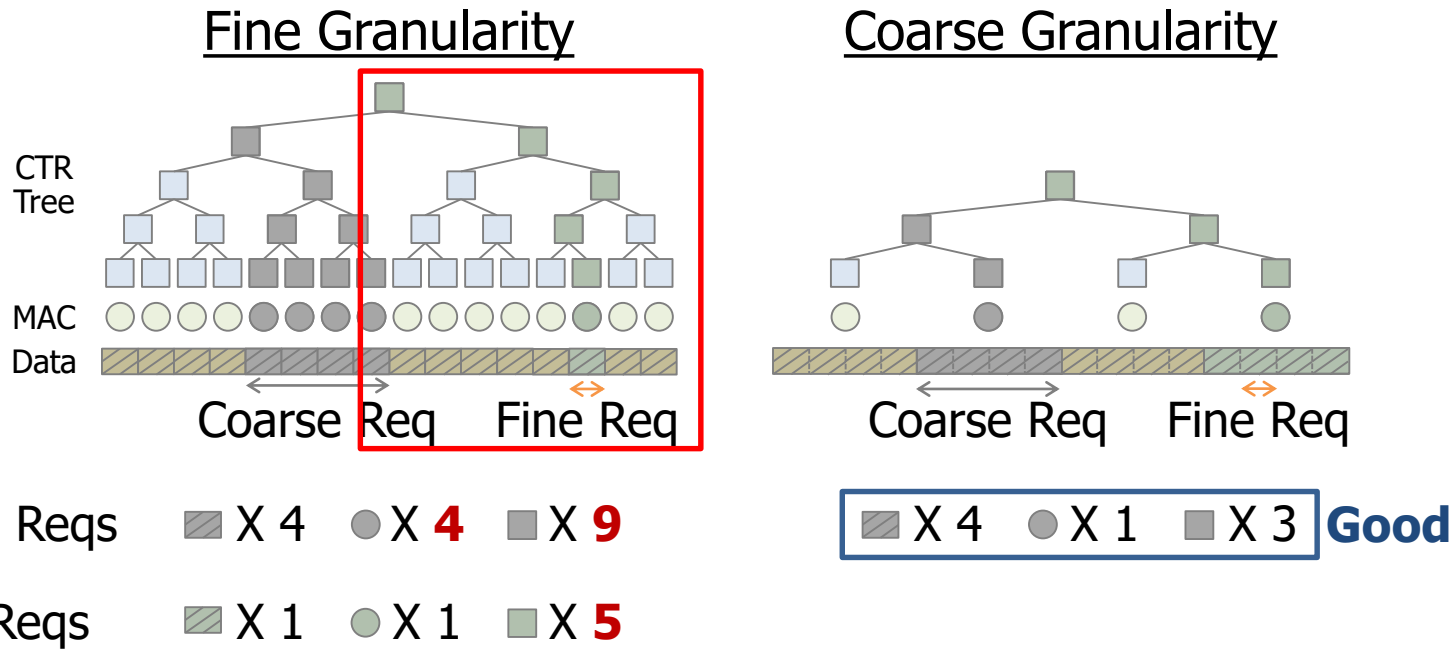

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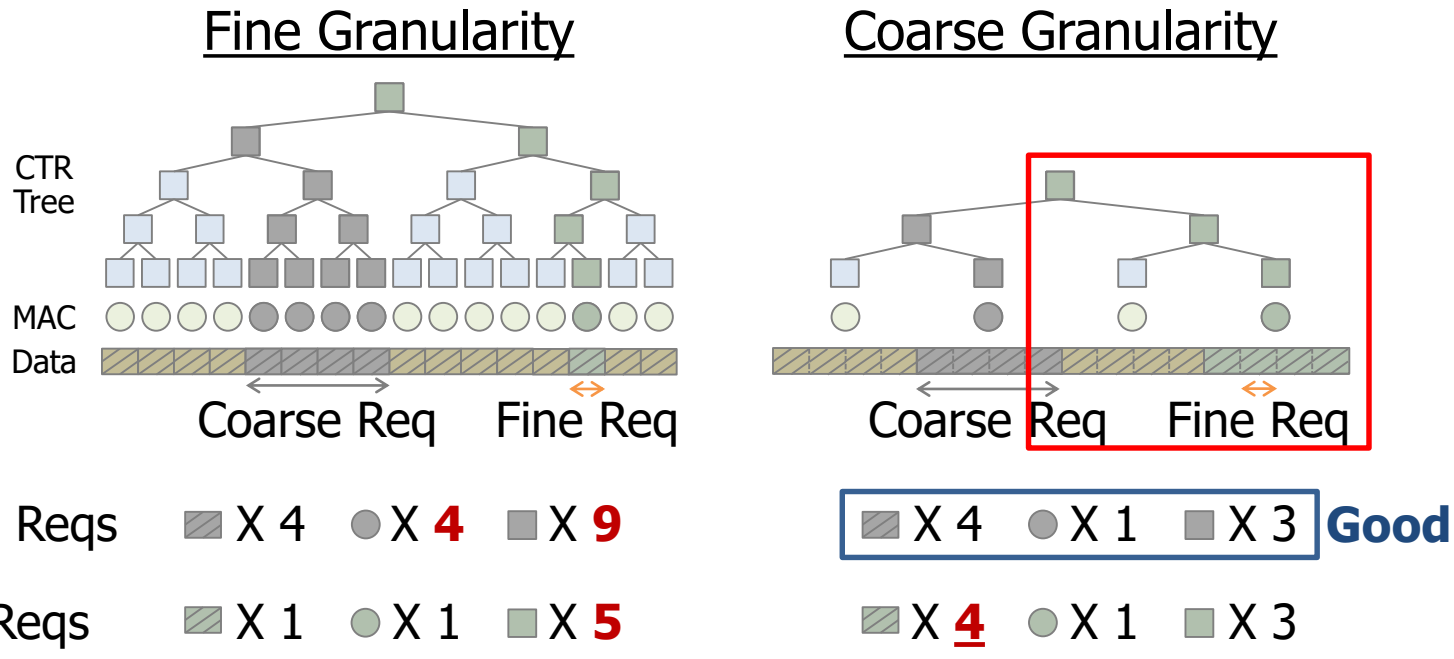

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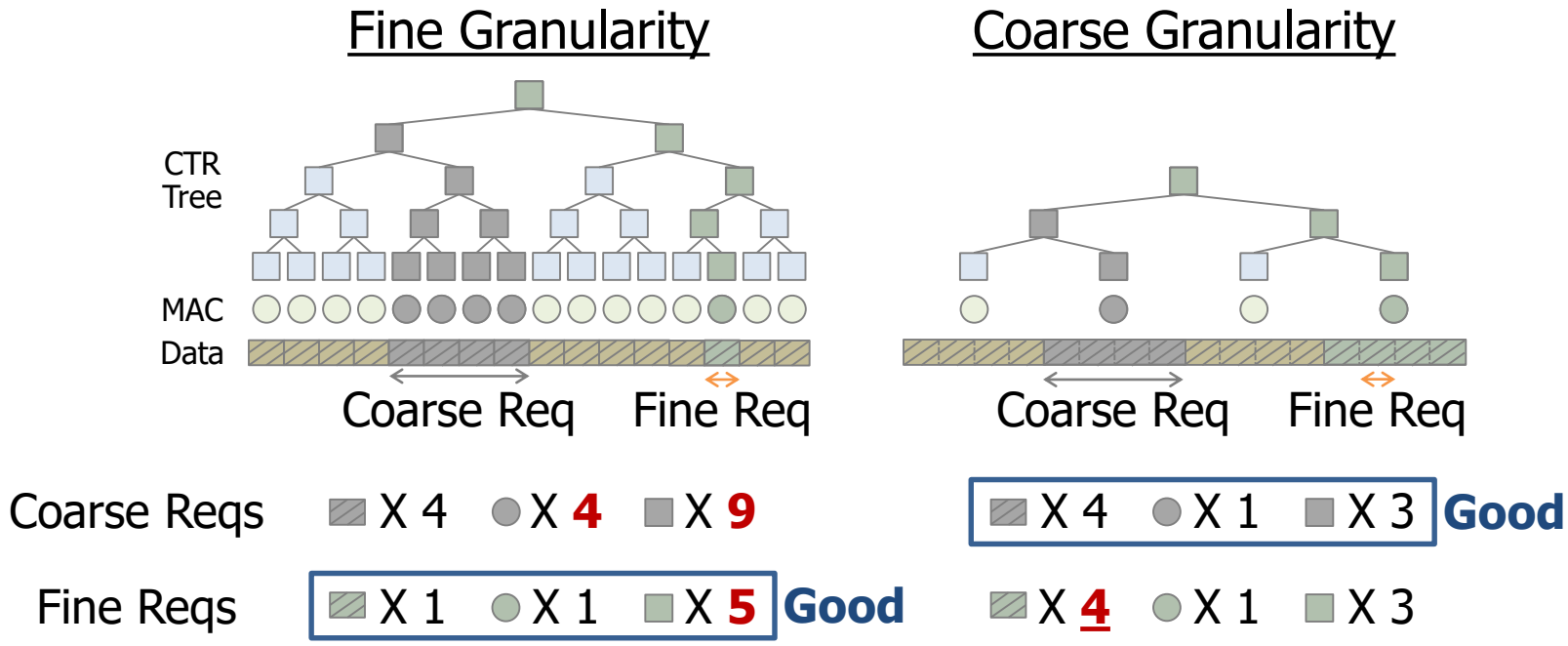

# Pros of Matching Granularity

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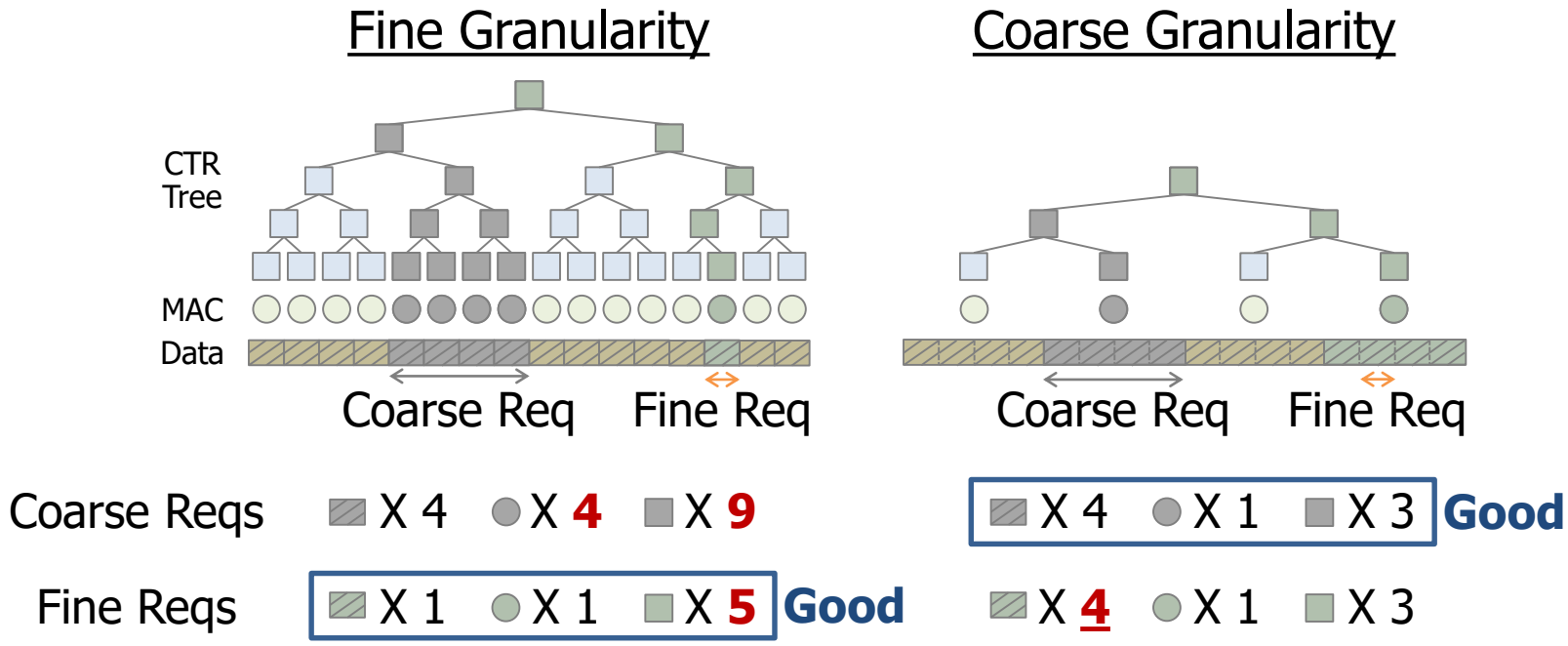


**Granularity-managed MAC&tree makes efficient memory protection**

# Prior Domain-specific Memory Protections

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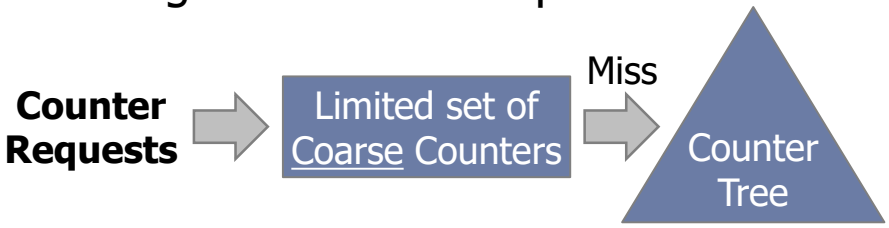


Dual CTRs, limited CTRs, CTR-only, device-specific

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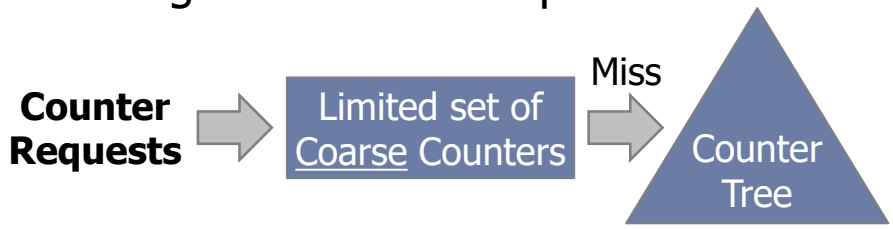


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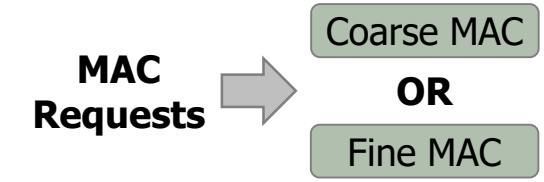


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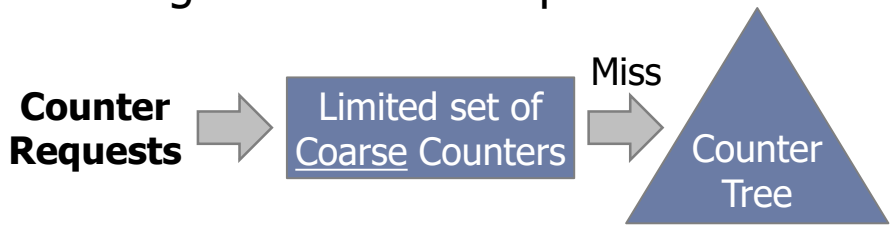


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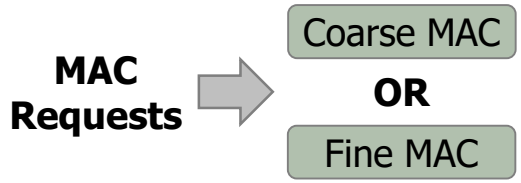
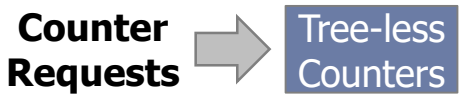



Dual MACs, MAC-only

3. S/W Counter [3-6]

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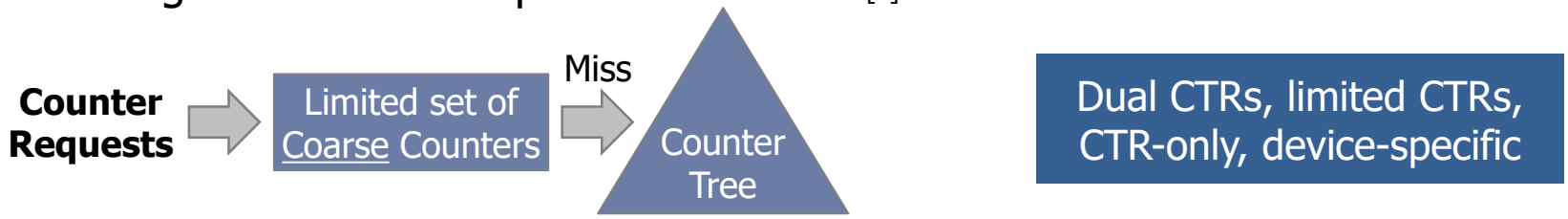


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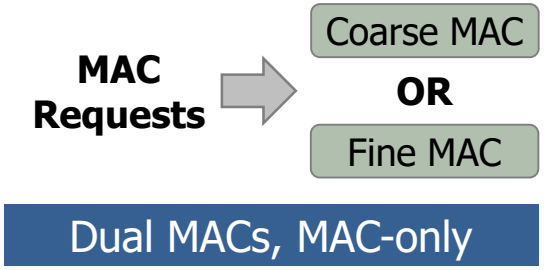


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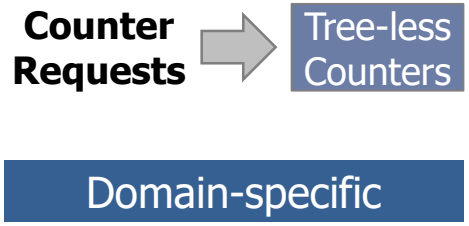


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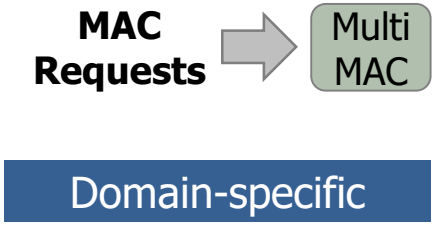



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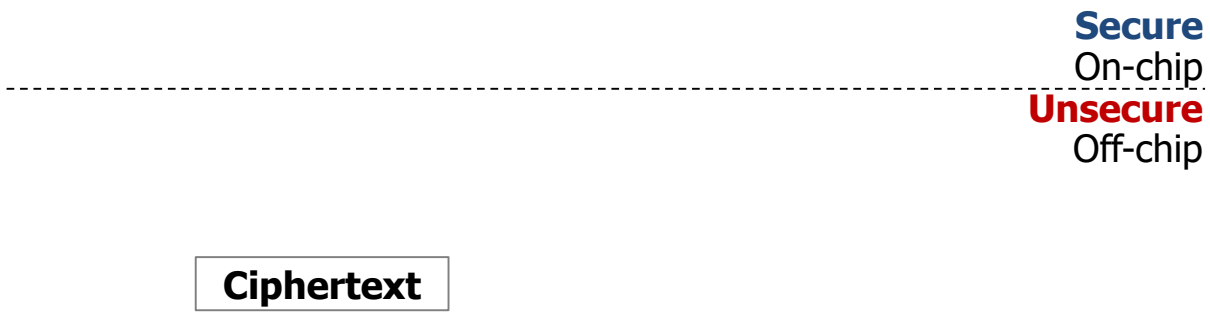

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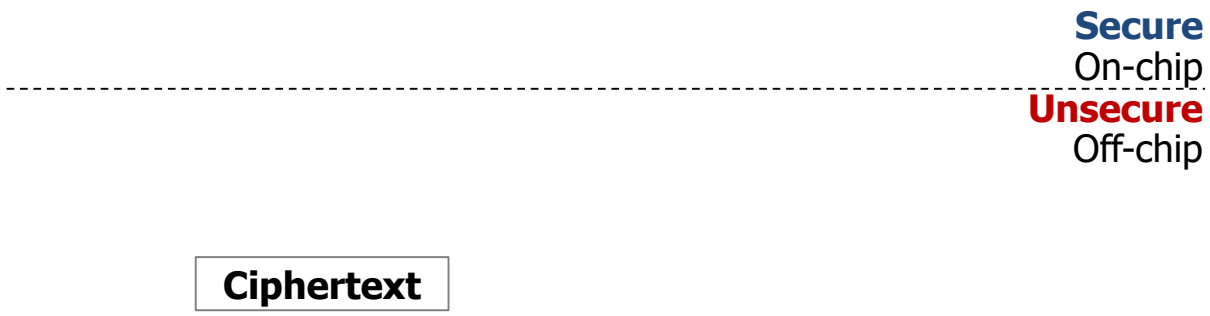

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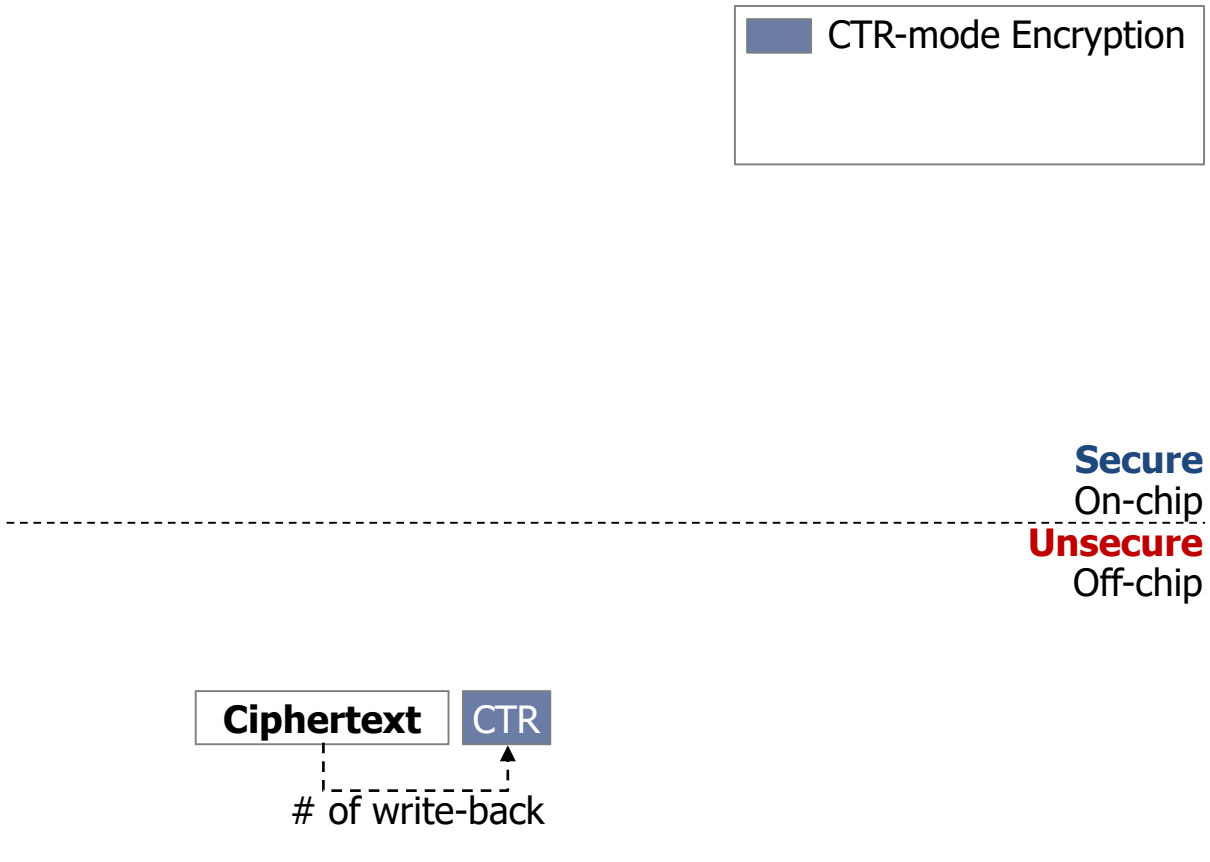

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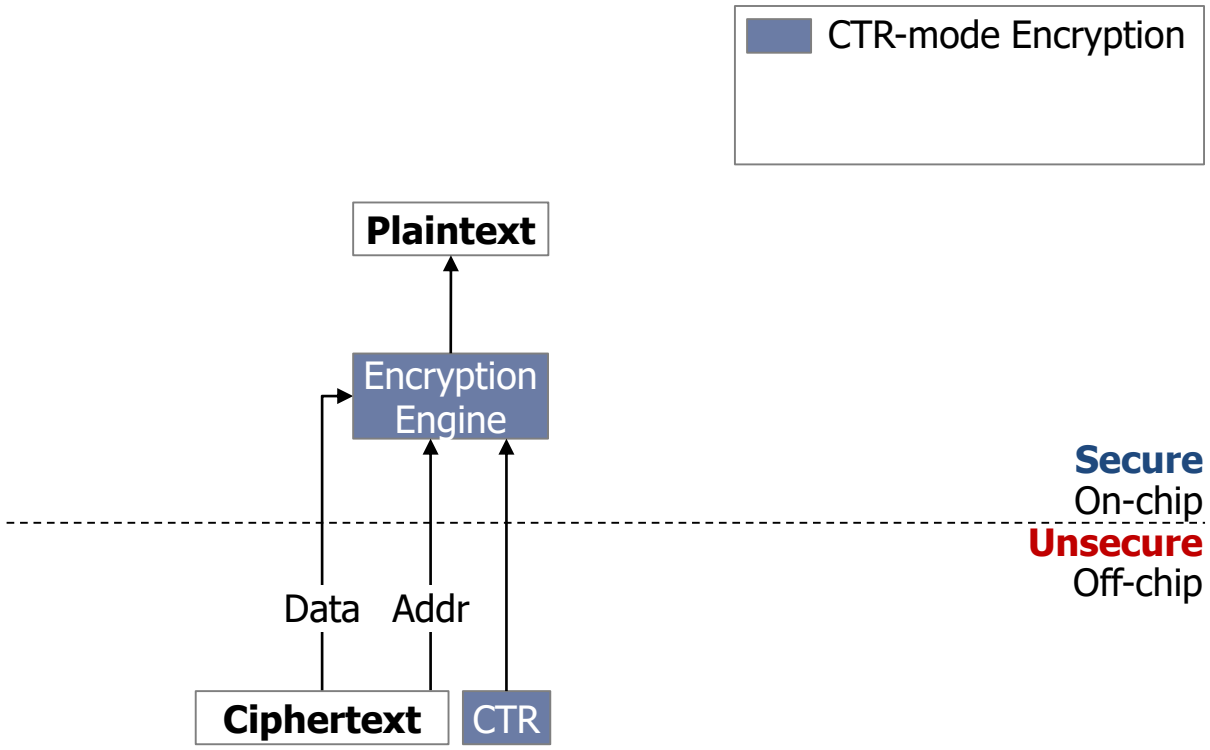

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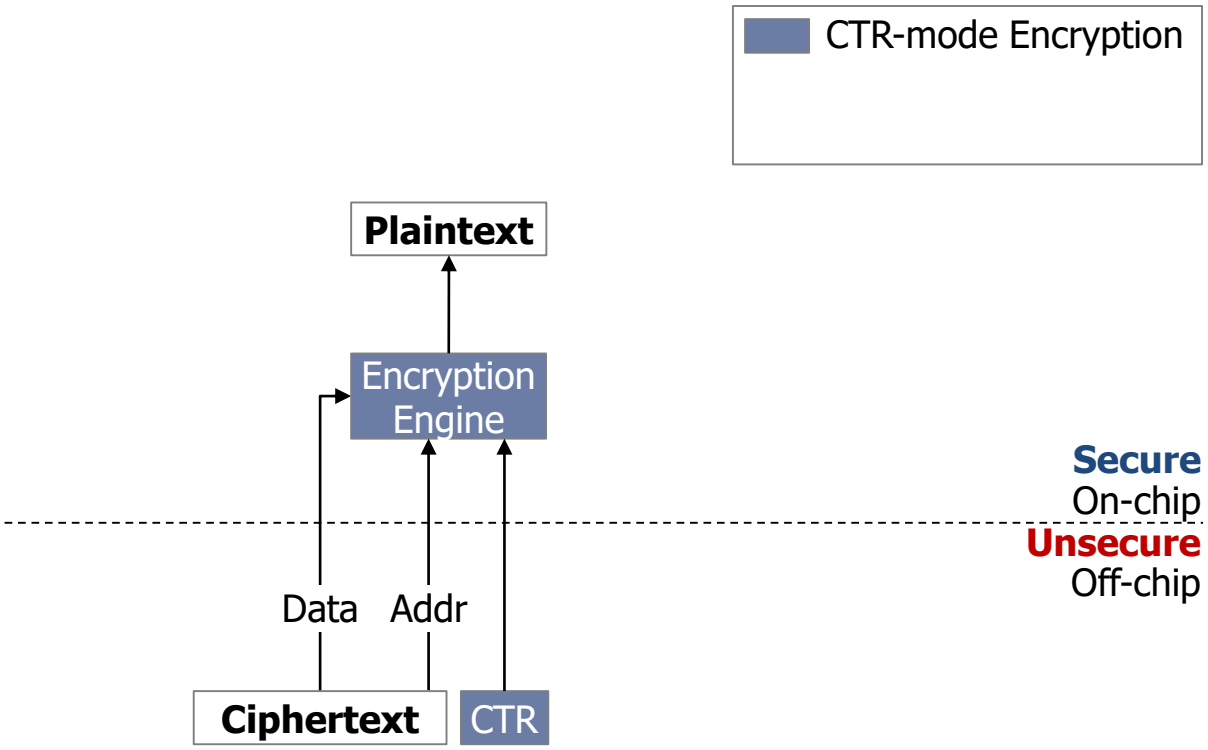

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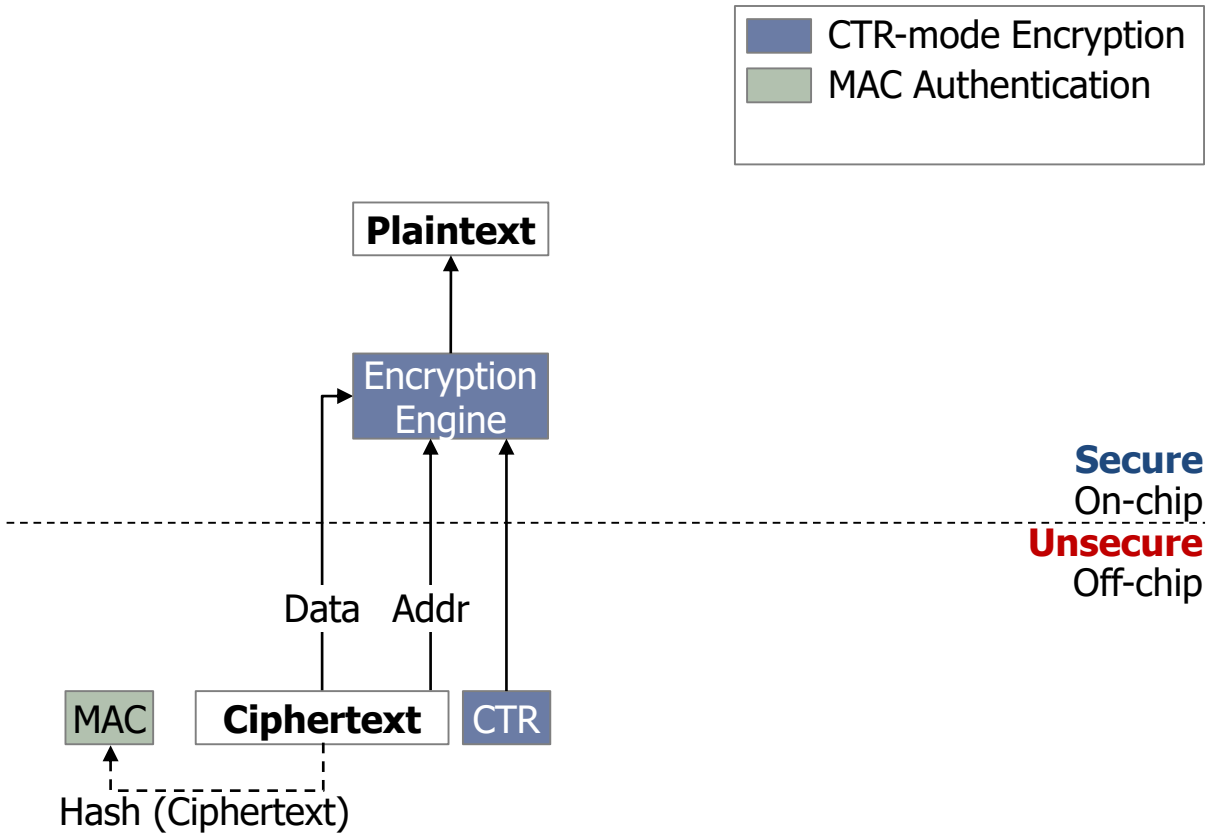

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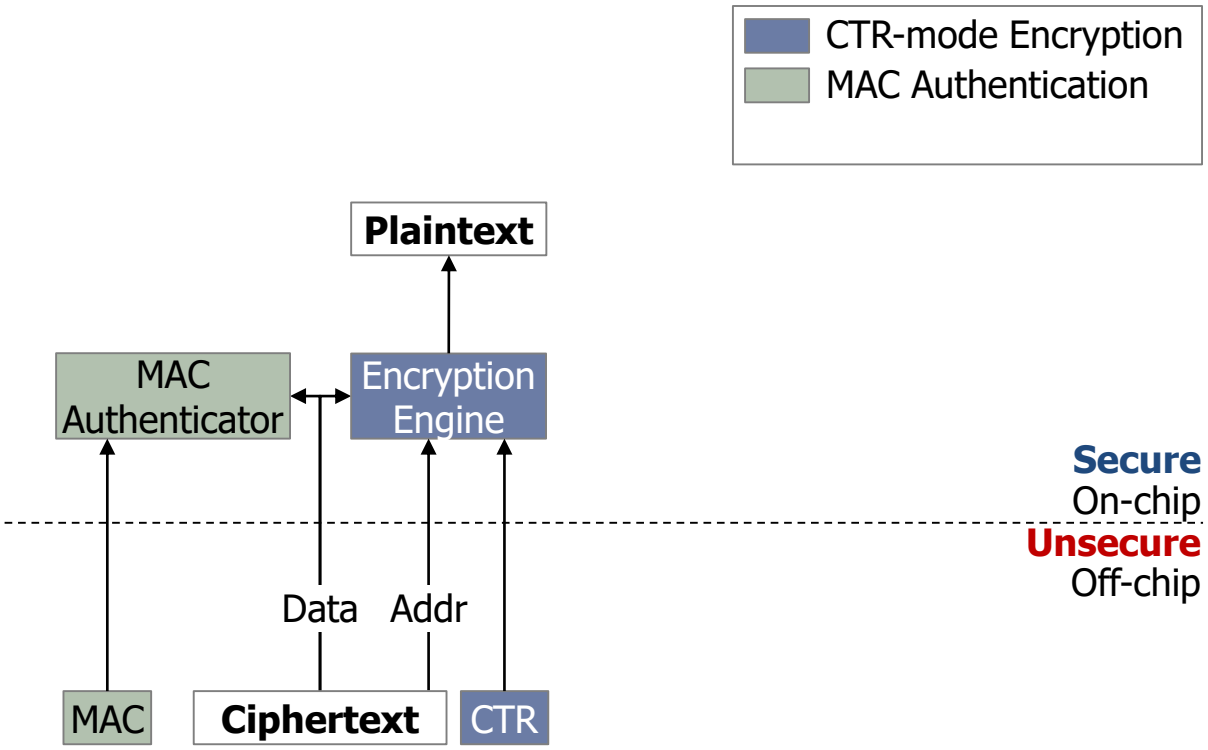

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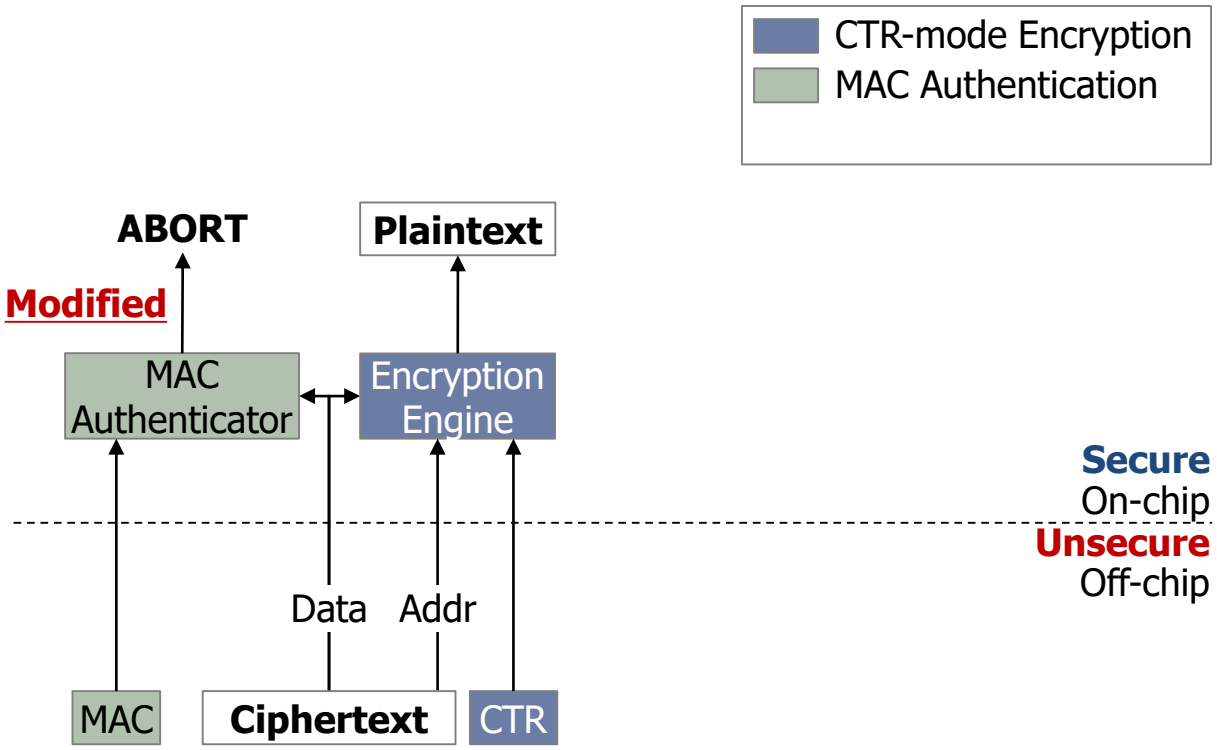

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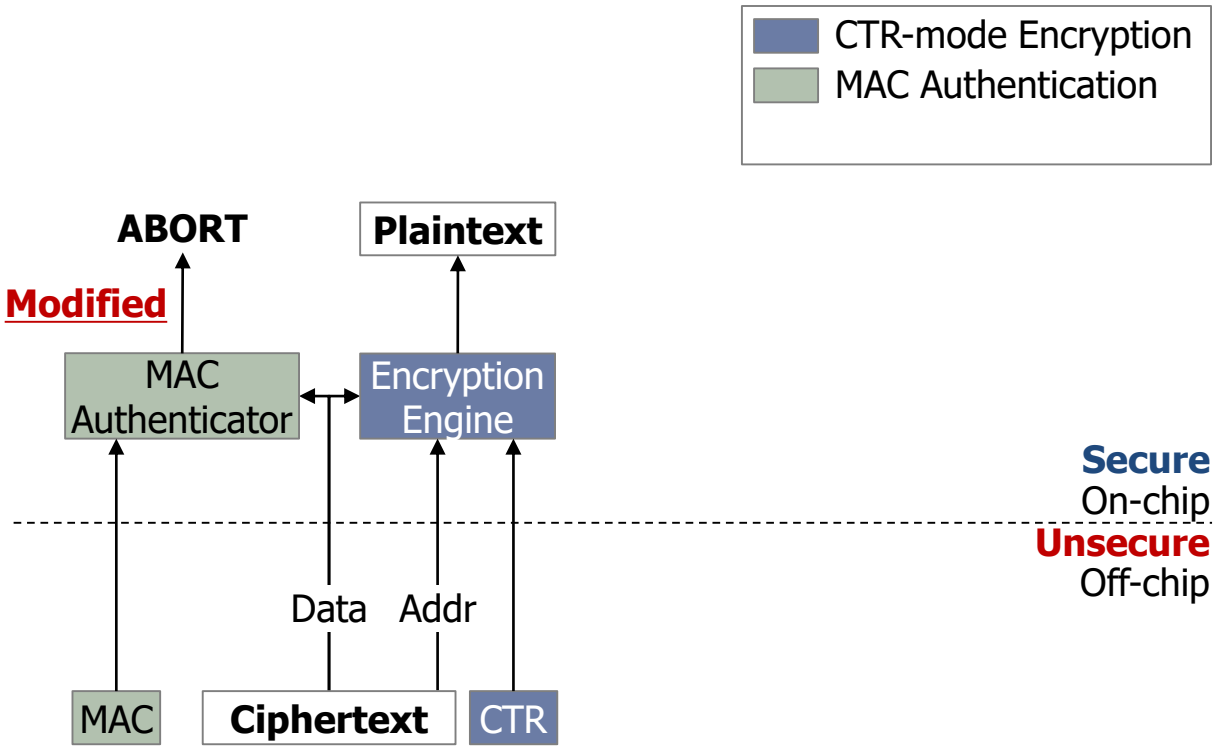

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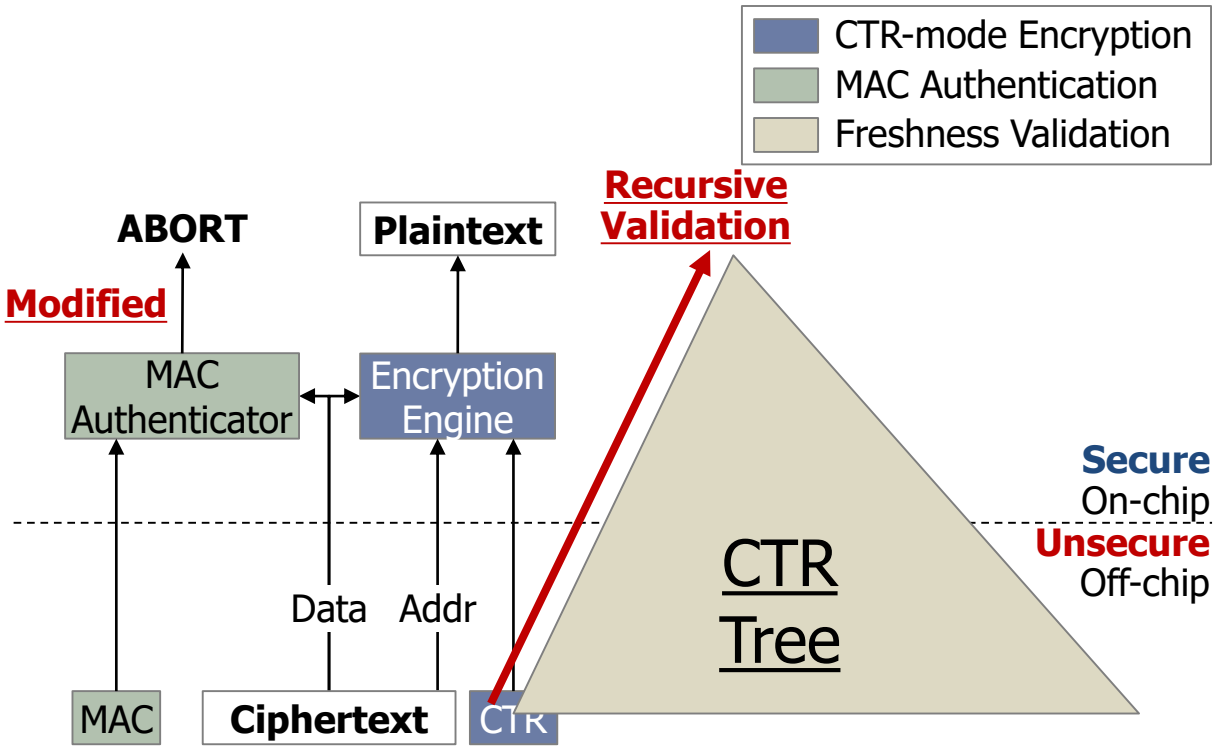

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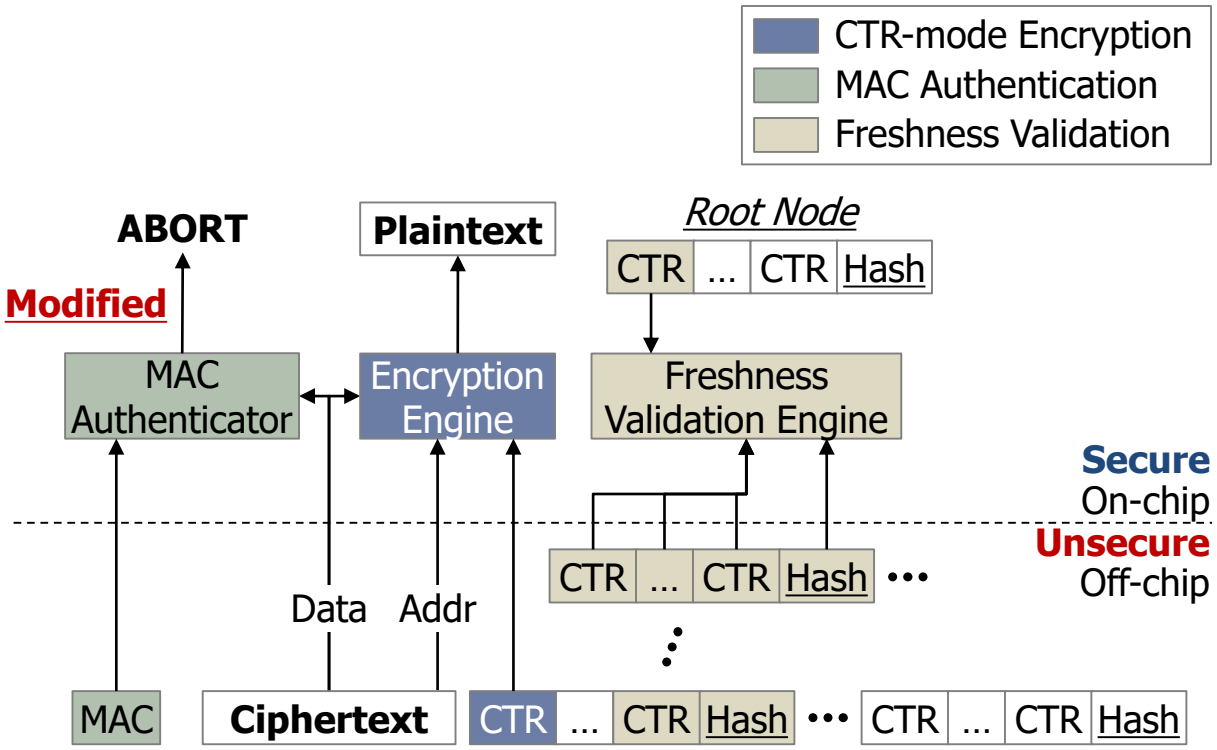

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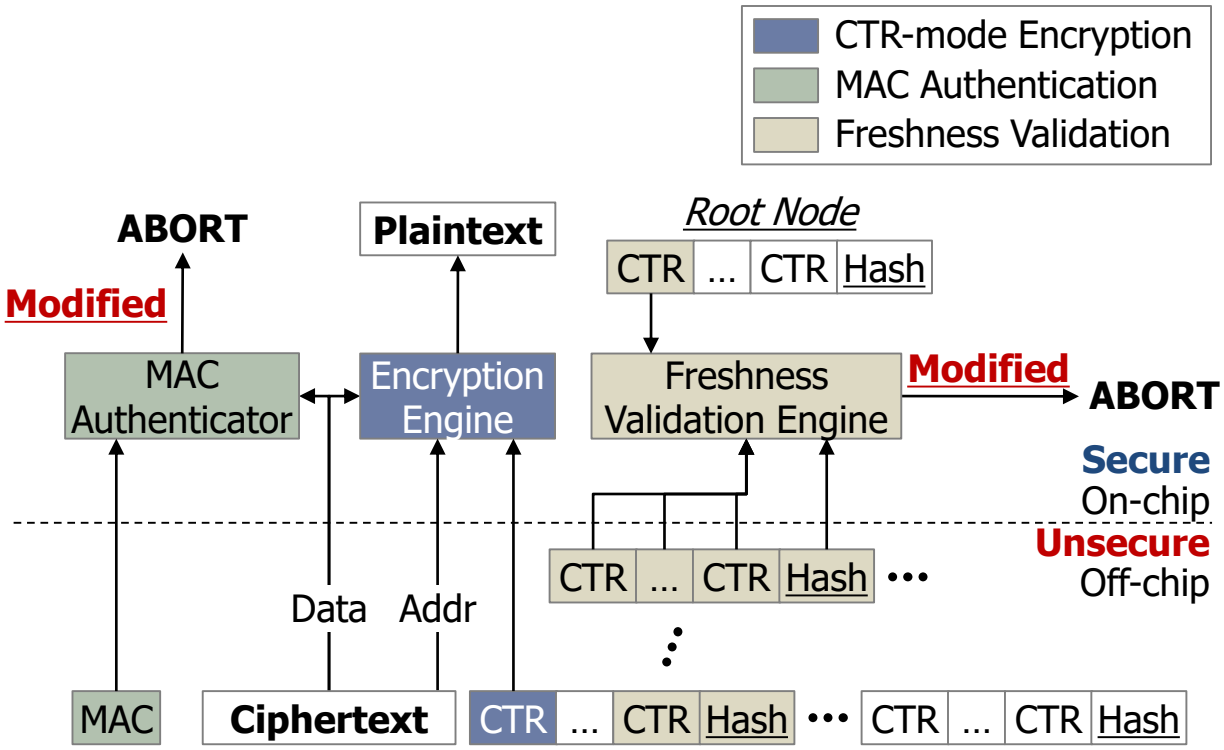

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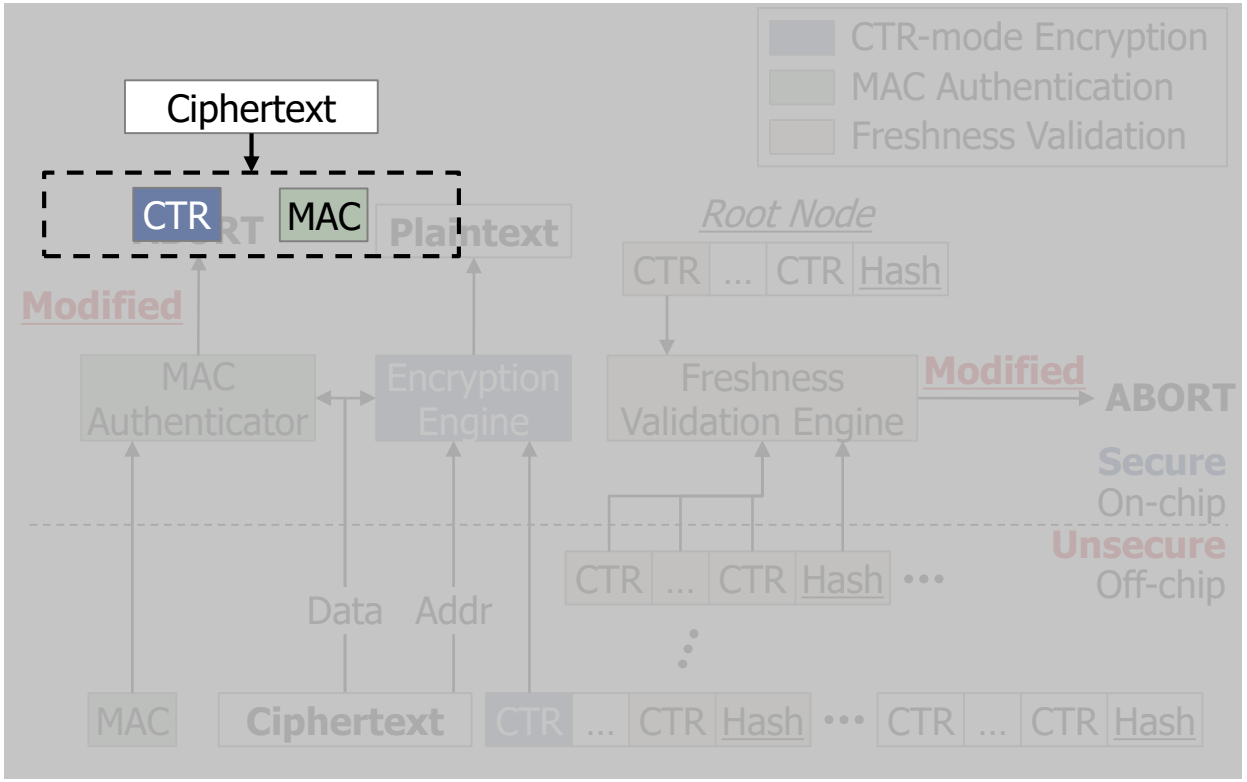

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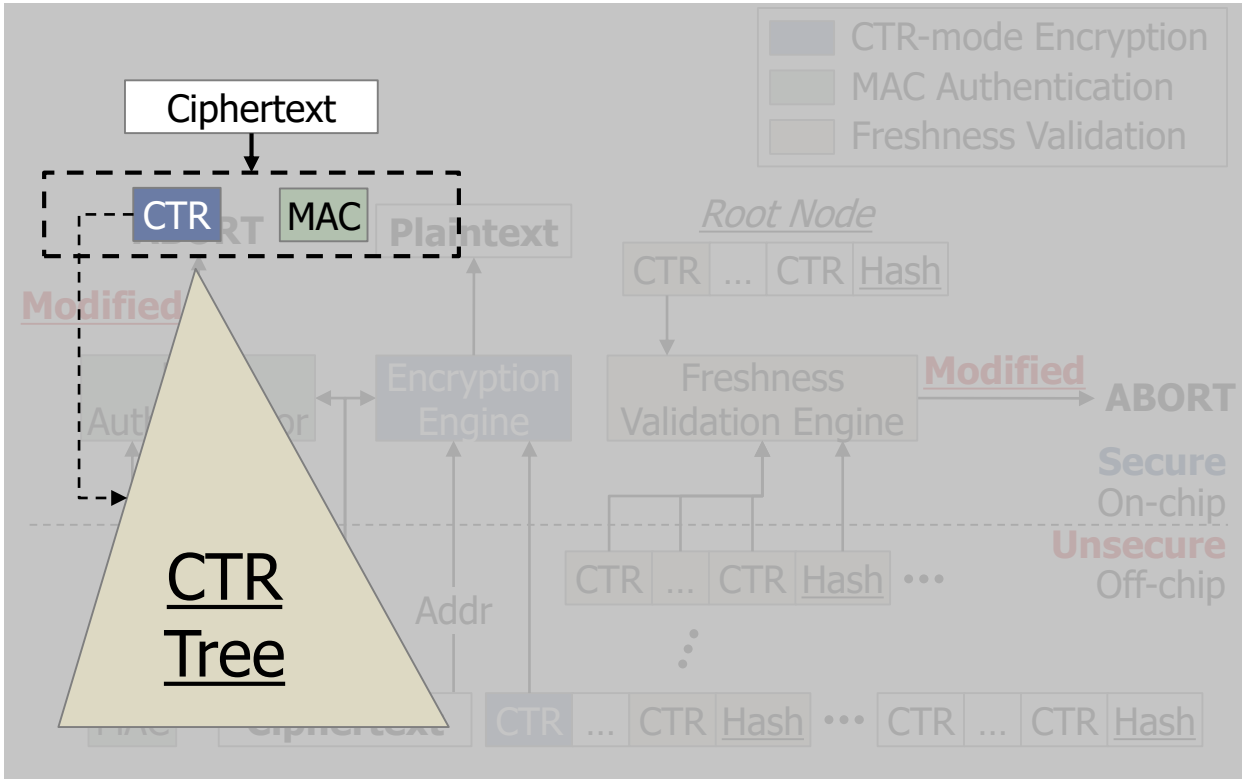

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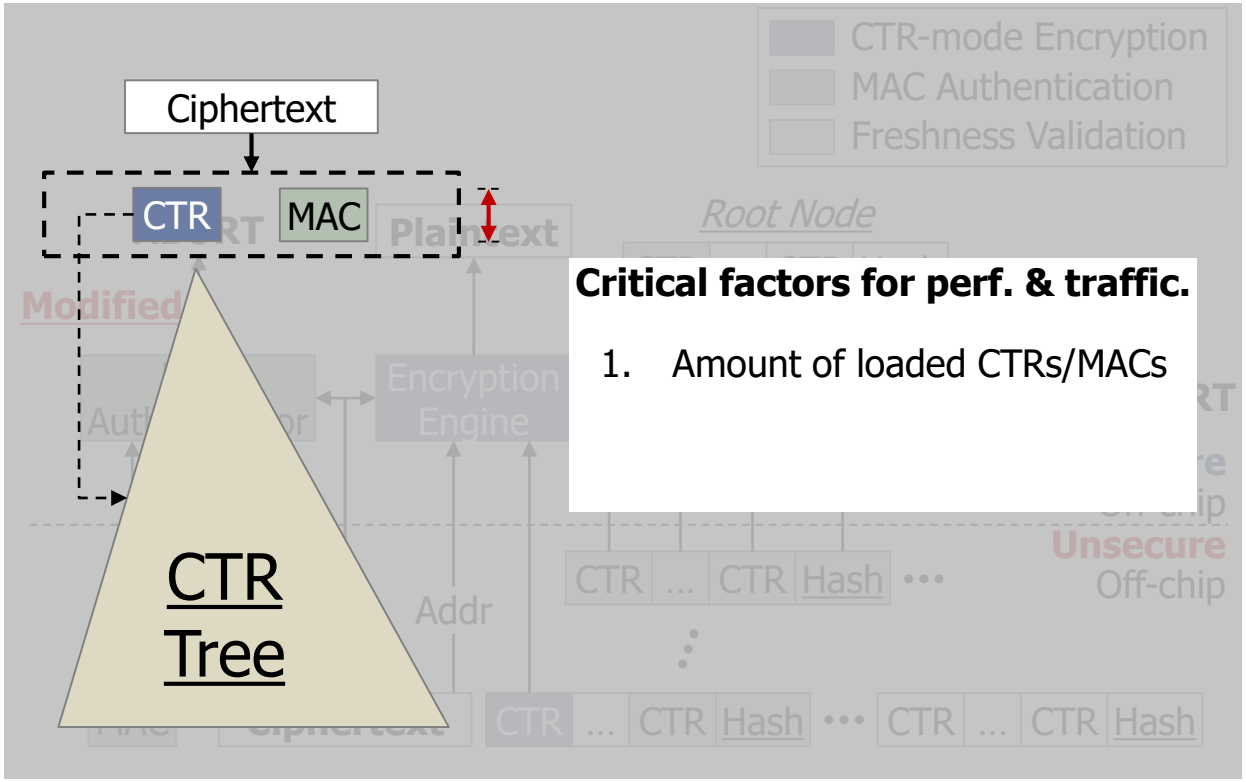


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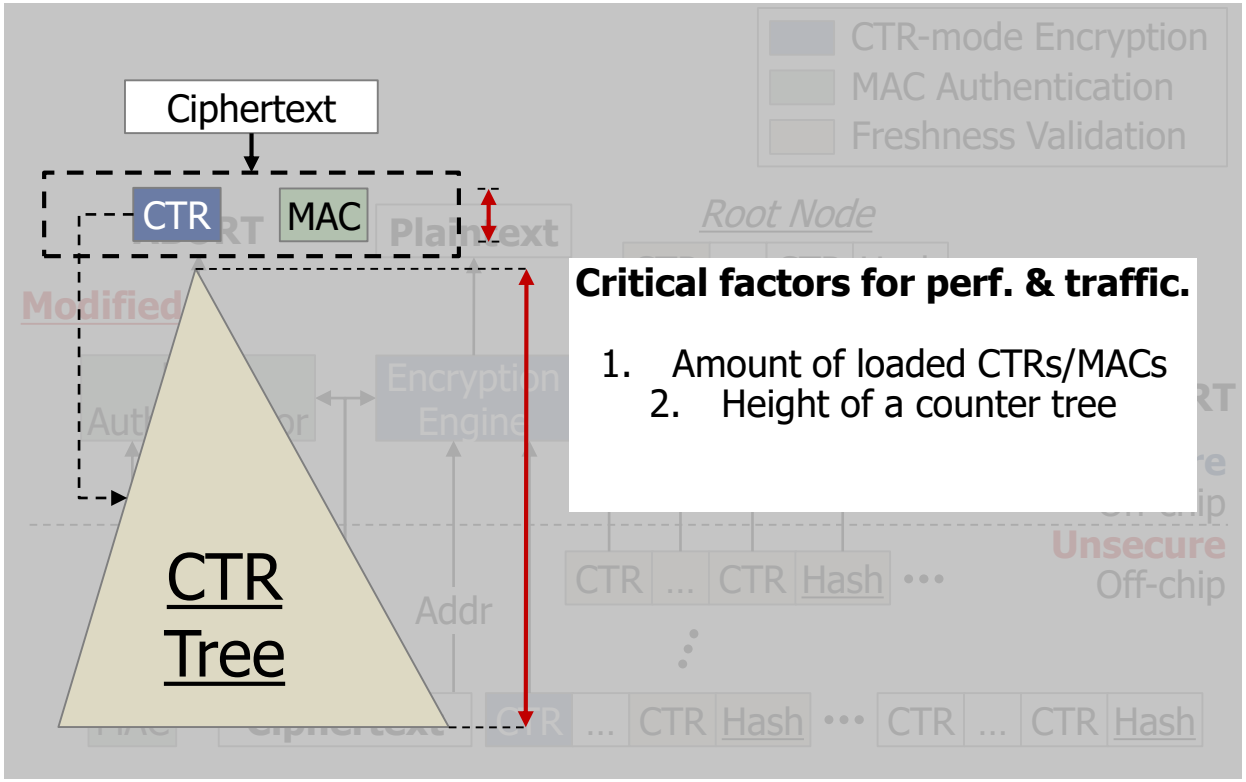


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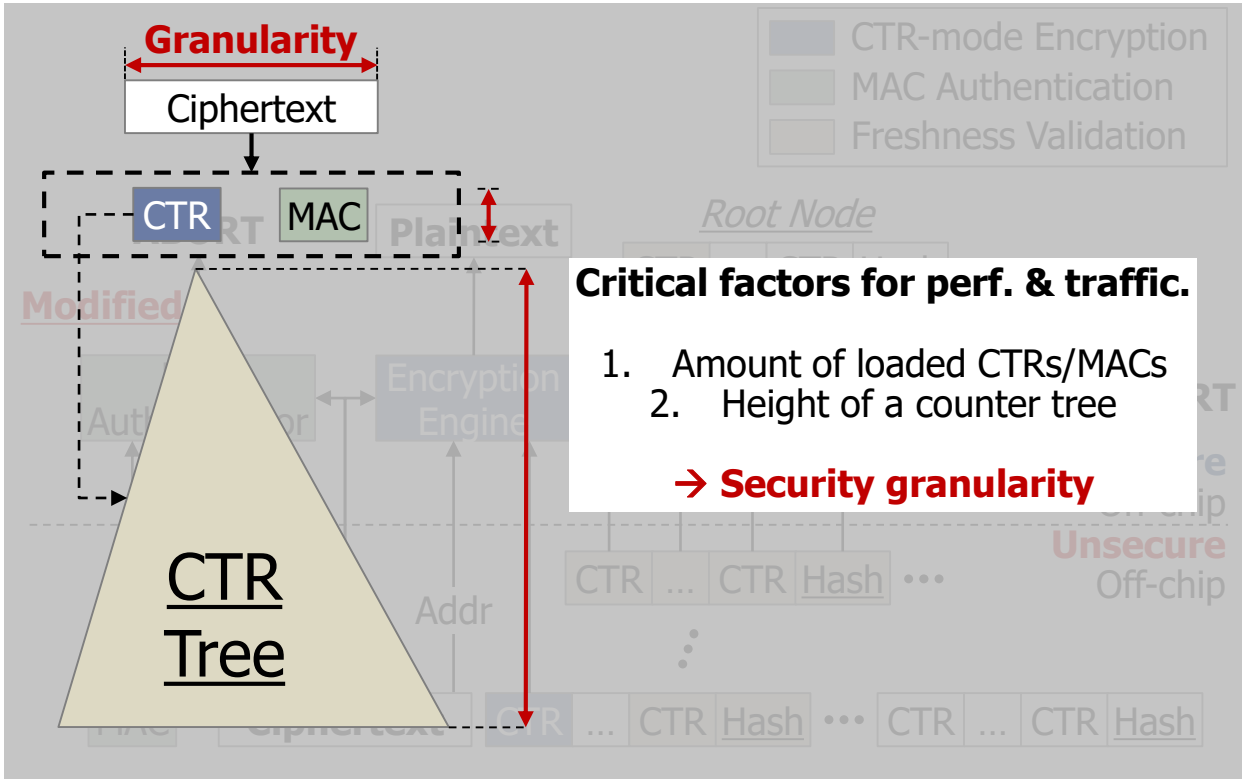

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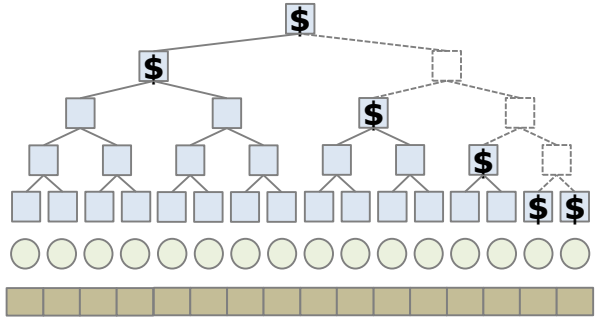
Prior Subtree Optimization

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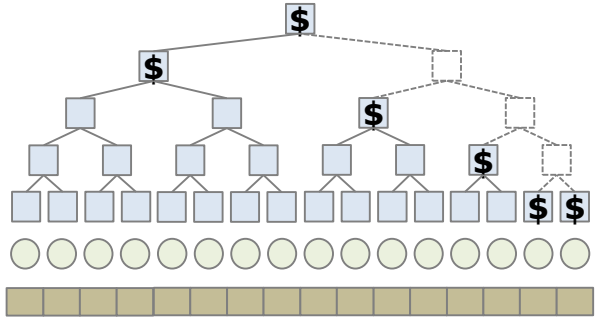


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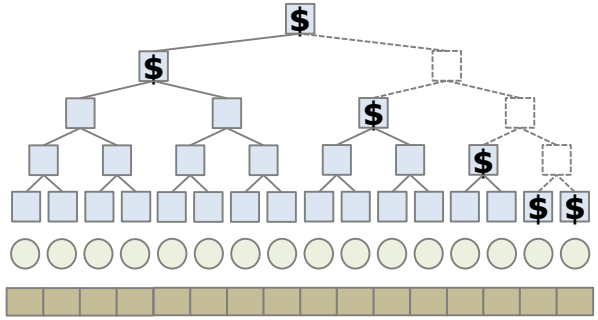


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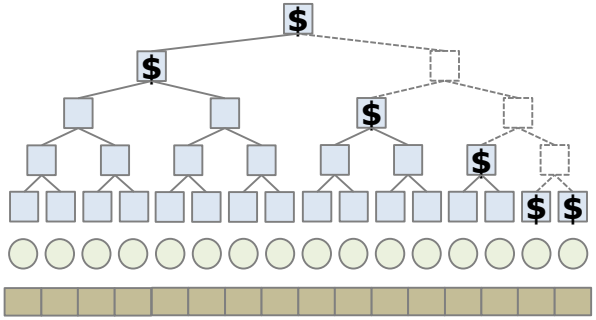
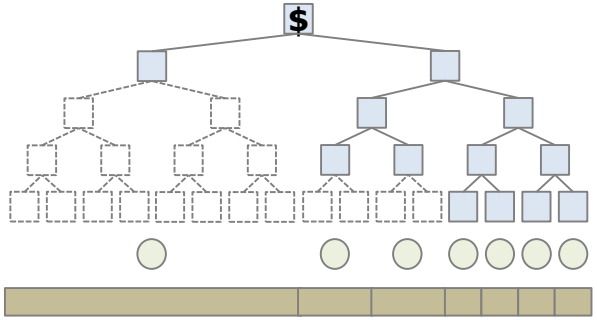



Ours





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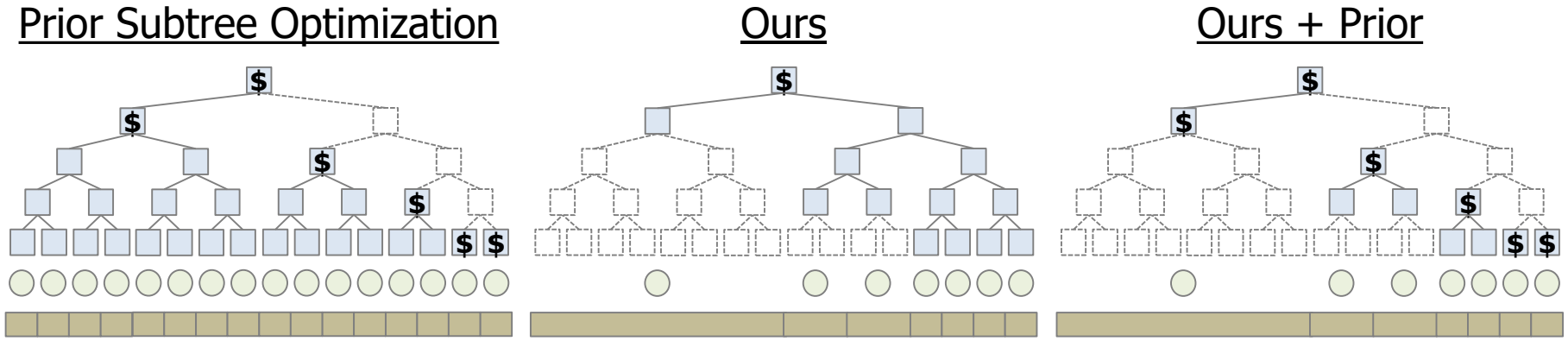



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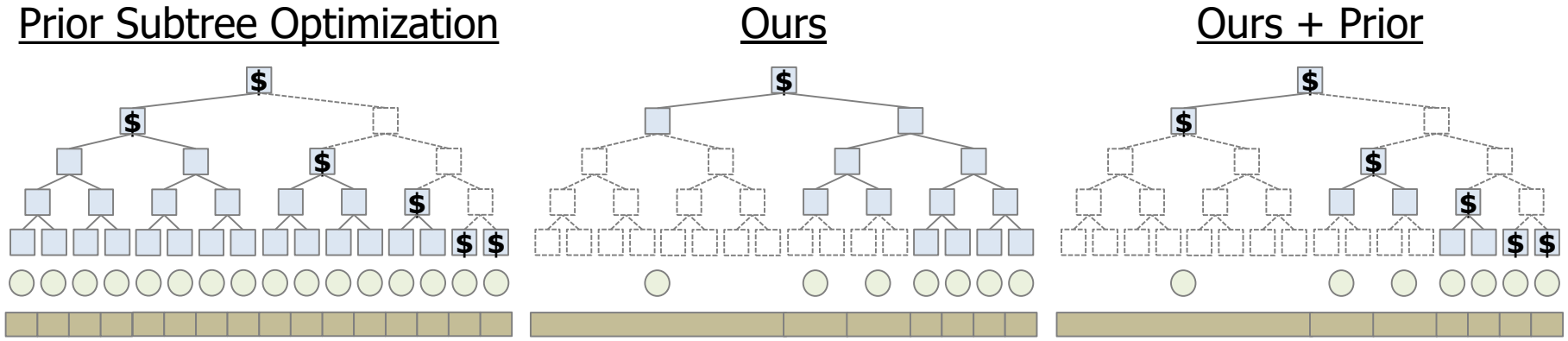


**Multi-granular MAC&Tree further improves prior solutions!!**

[4] Data Enclave: A Data-Centric Trusted Execution Environment (HPCA 2024)

# Design of Multi-granular MAC&Tree

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1. Granularity Switching

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1. Granularity Switching
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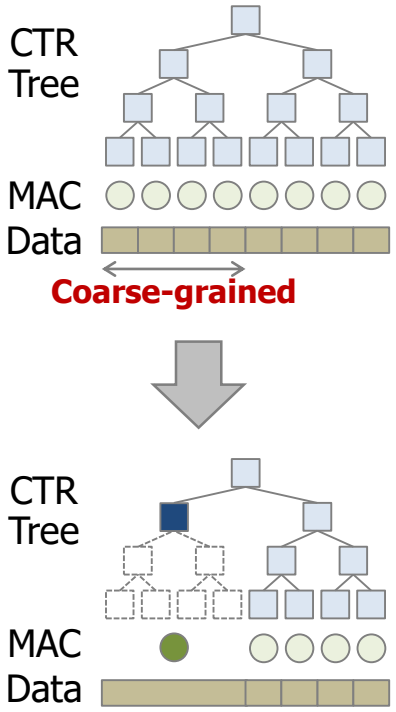


MAC/CTR Merging
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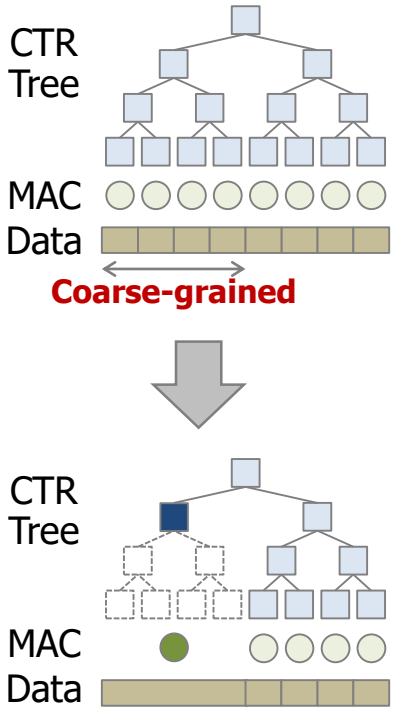


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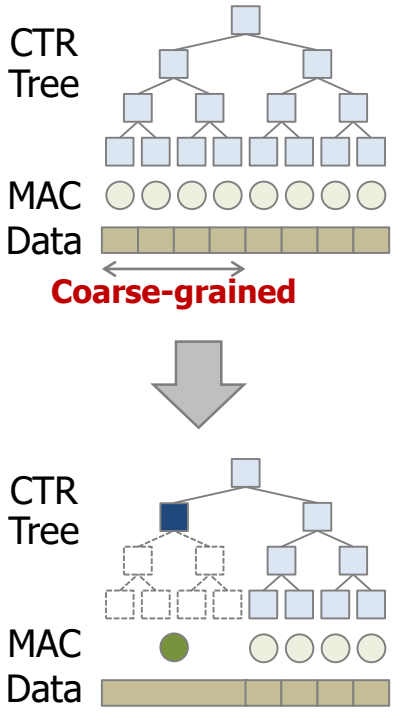


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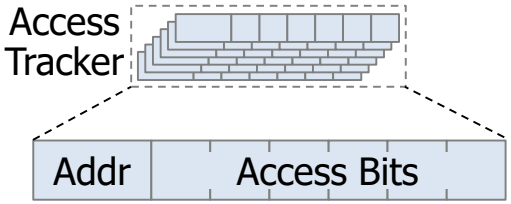


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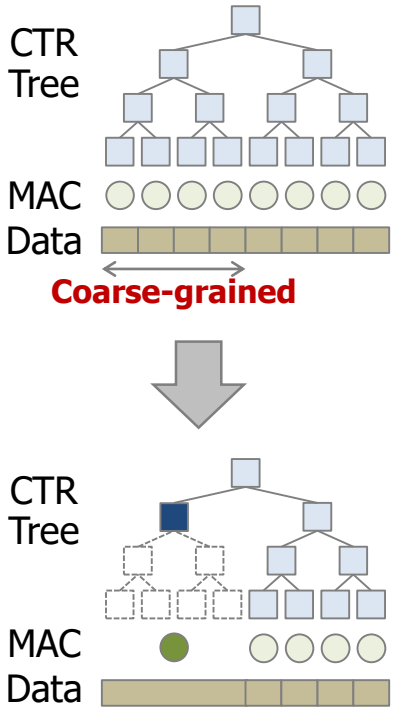


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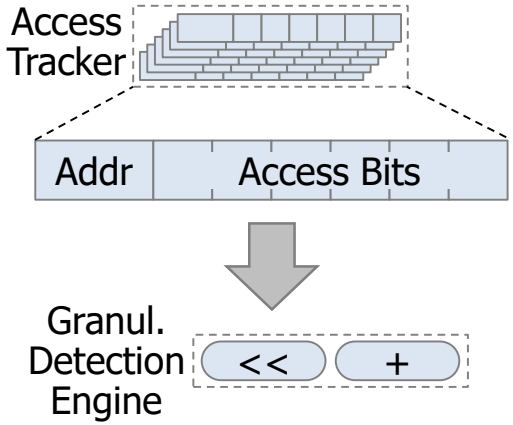


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# Design of Multi-granular MAC&Tree

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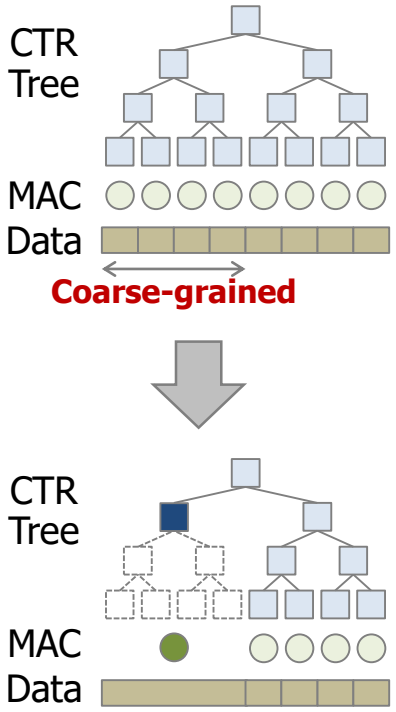
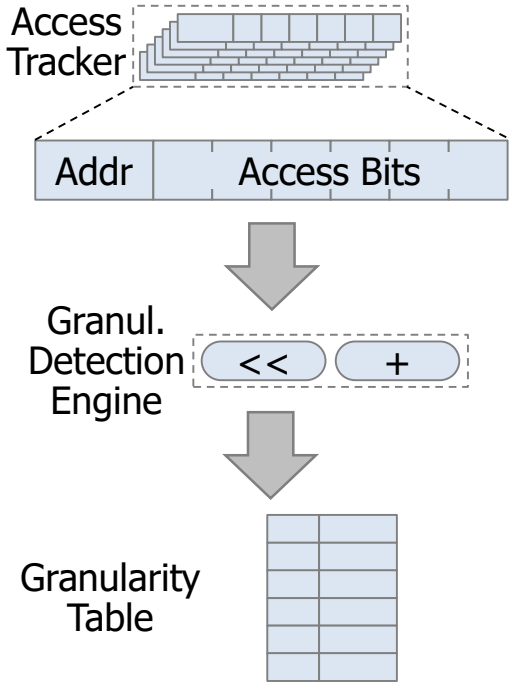



MAC/CTR Merging
& CTR Tree Pruning

2. Granularity Detection




Dynamic Access Tracking

3. Multi-granularity
Memory Protection

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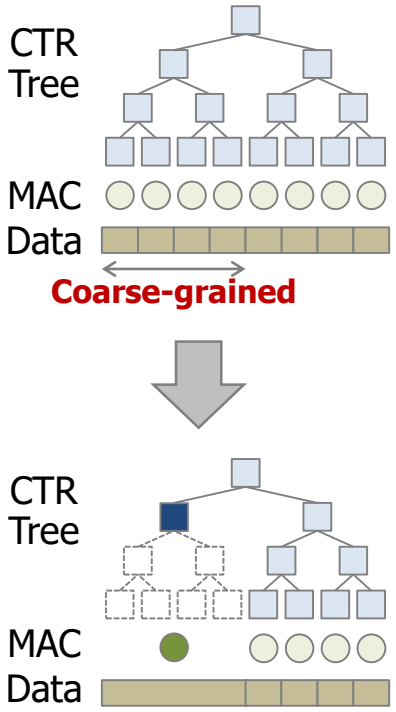


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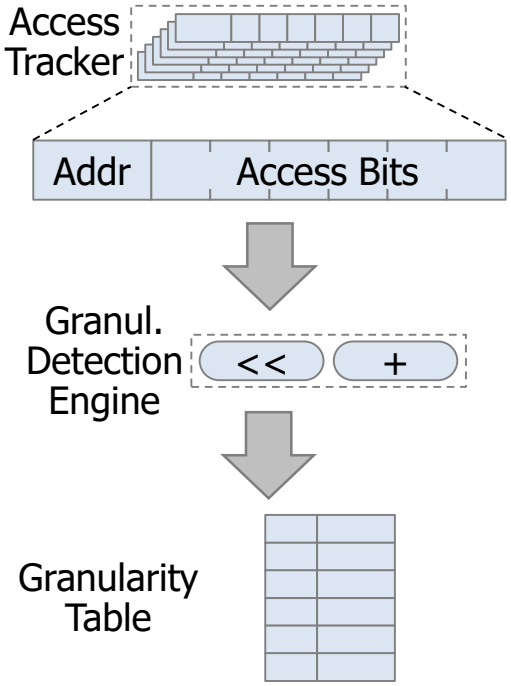


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Granularity-aware Protection

# Design of Multi-granular MAC&Tree

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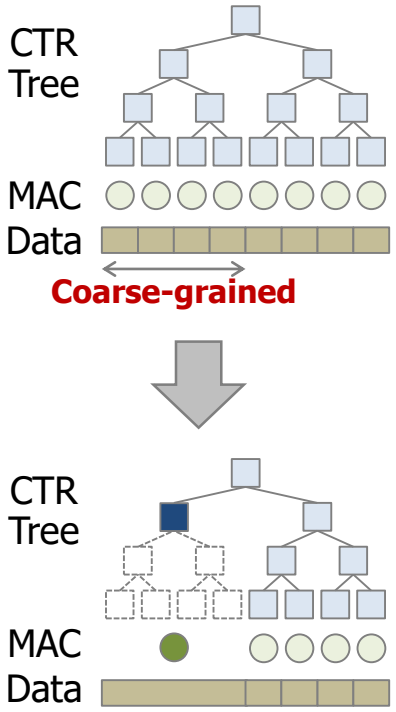


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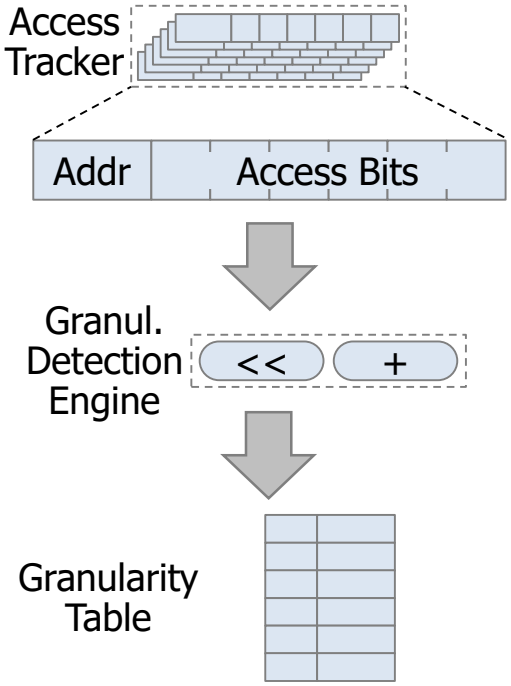
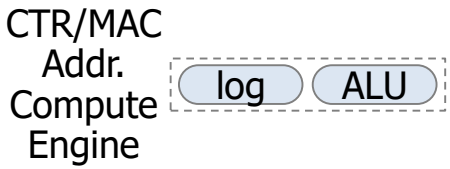



Dynamic Access Tracking

3. Multi-granularity Memory Protection




Granularity-aware Protection

Backup

# Design of Multi-granular MAC&Tree

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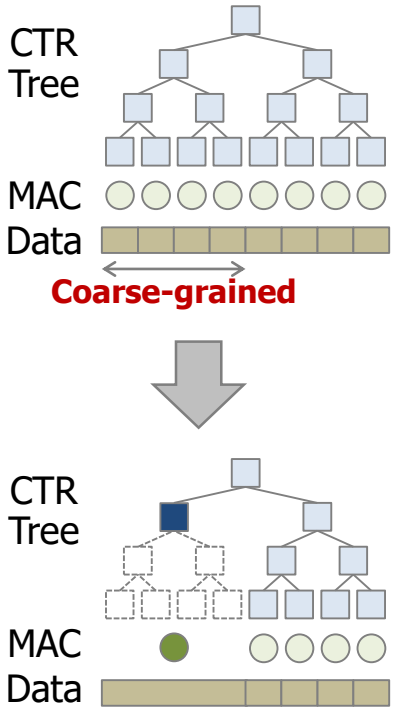


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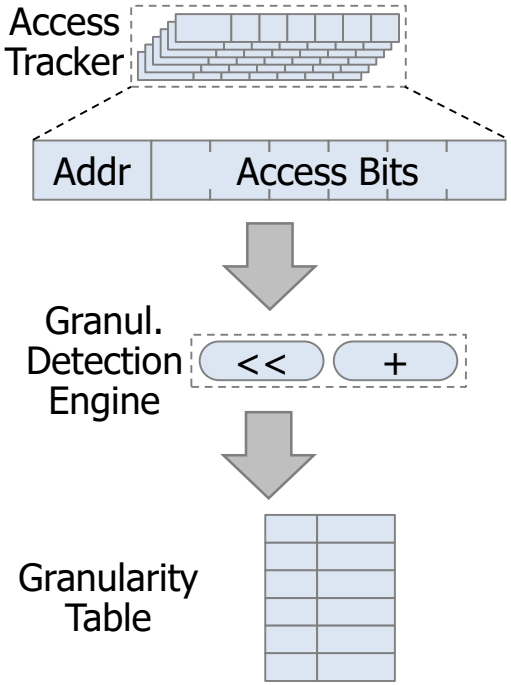
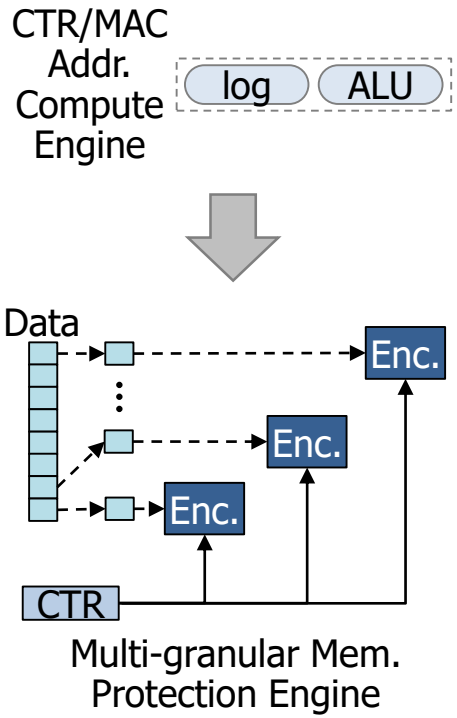



Dynamic Access Tracking

## 3. Multi-granularity Memory Protection




Granularity-aware Protection

# Design of Multi-granular MAC&Tree

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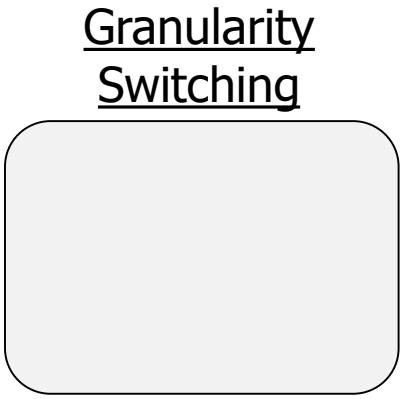

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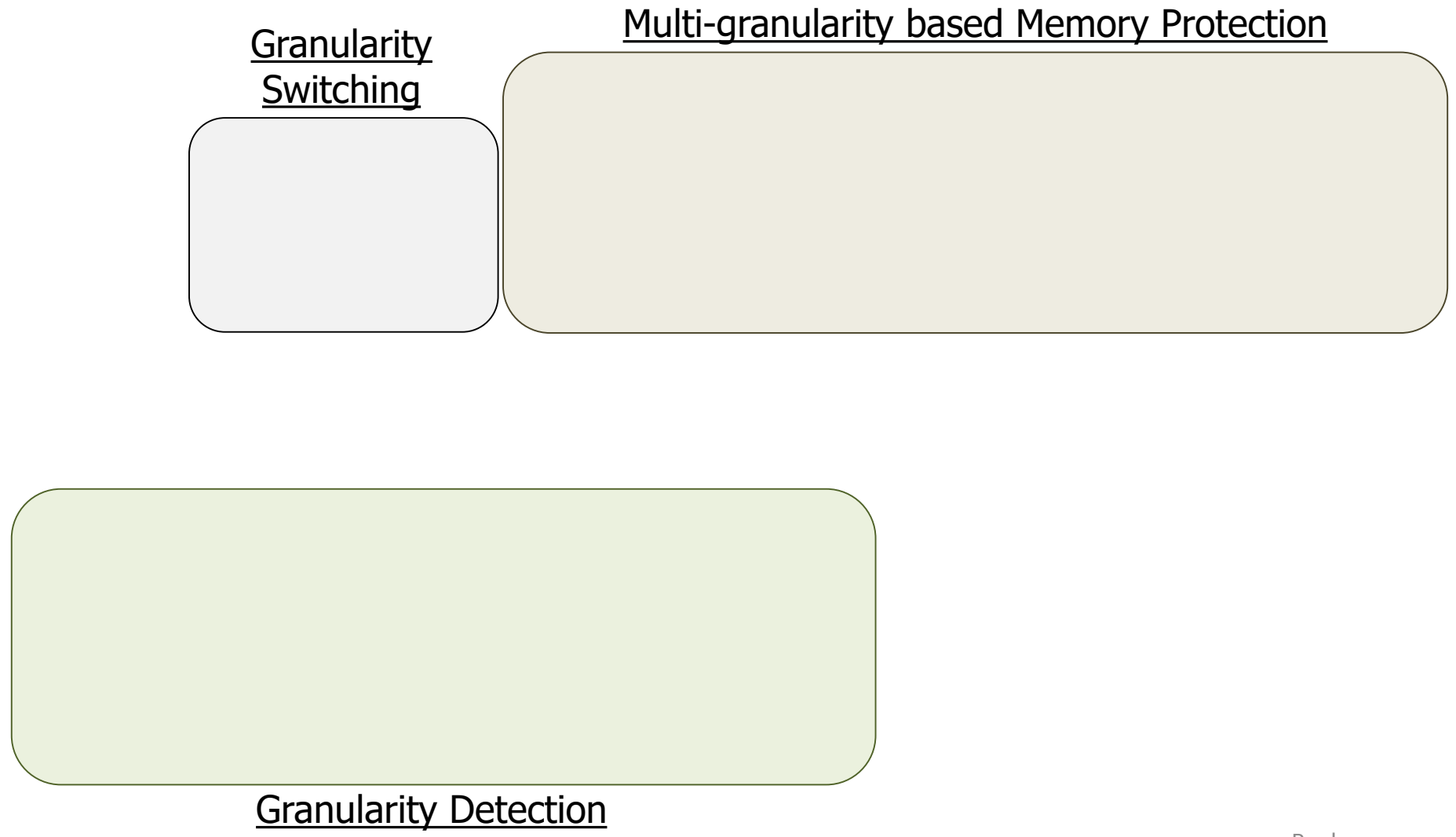

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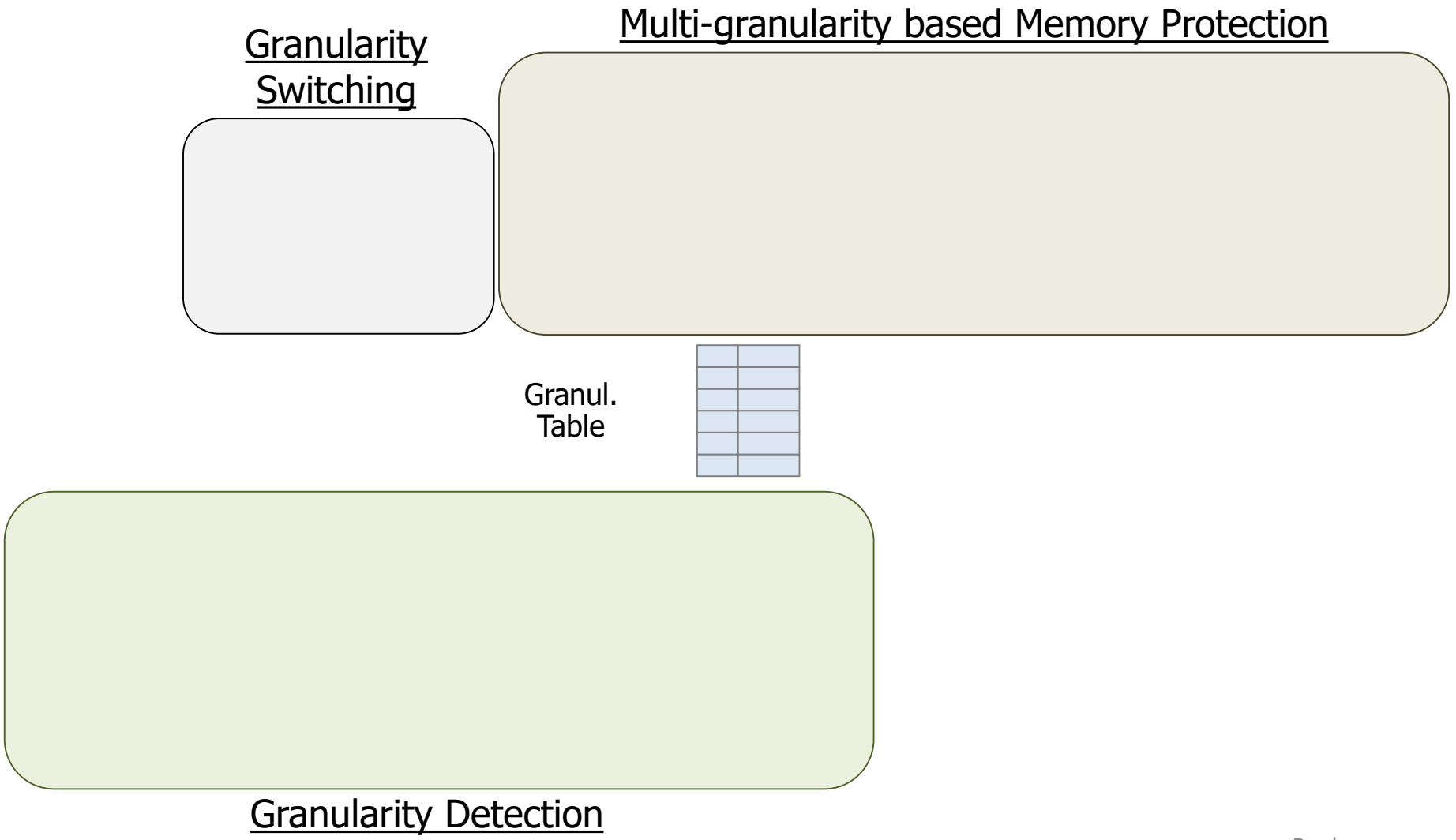

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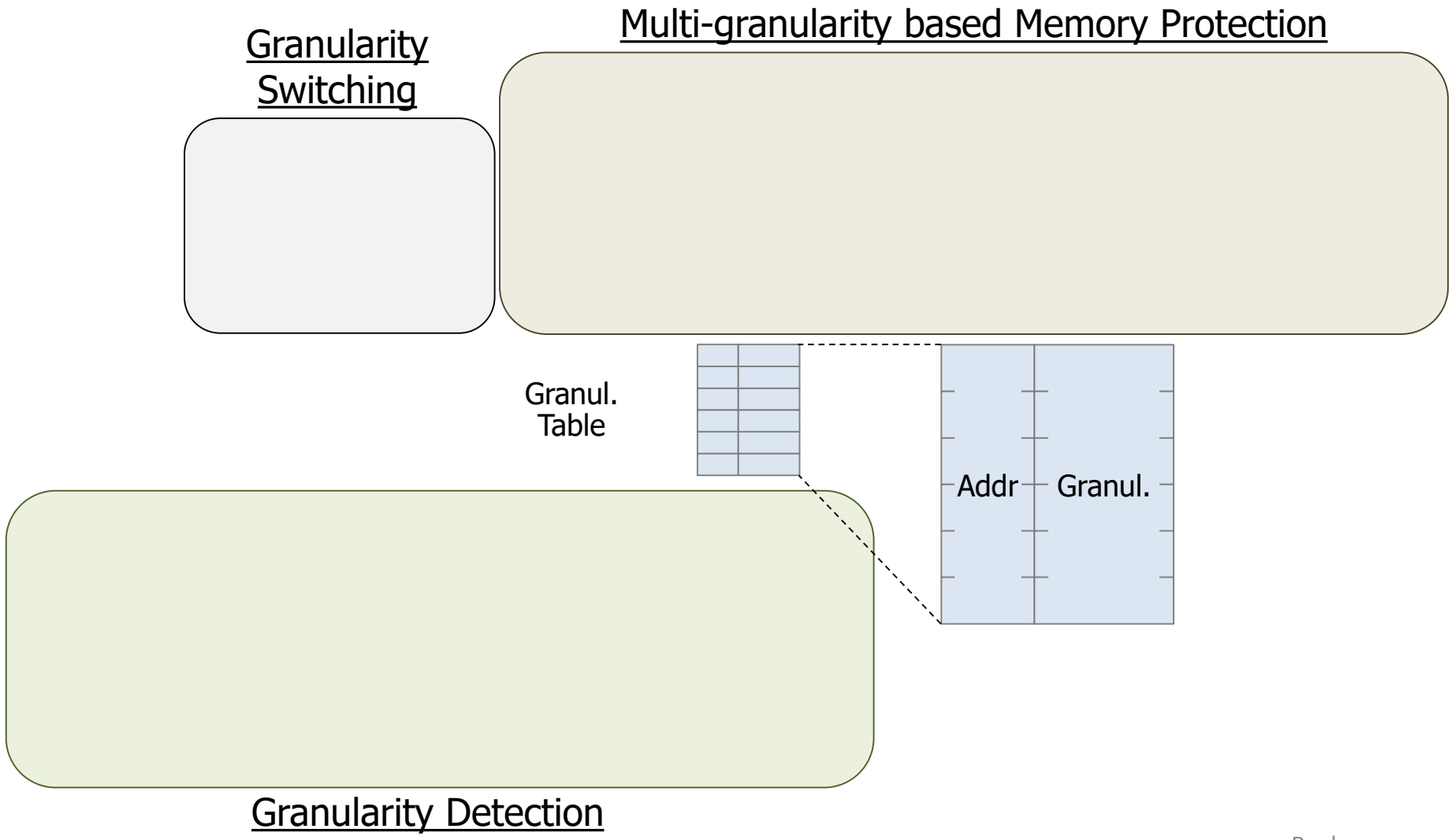

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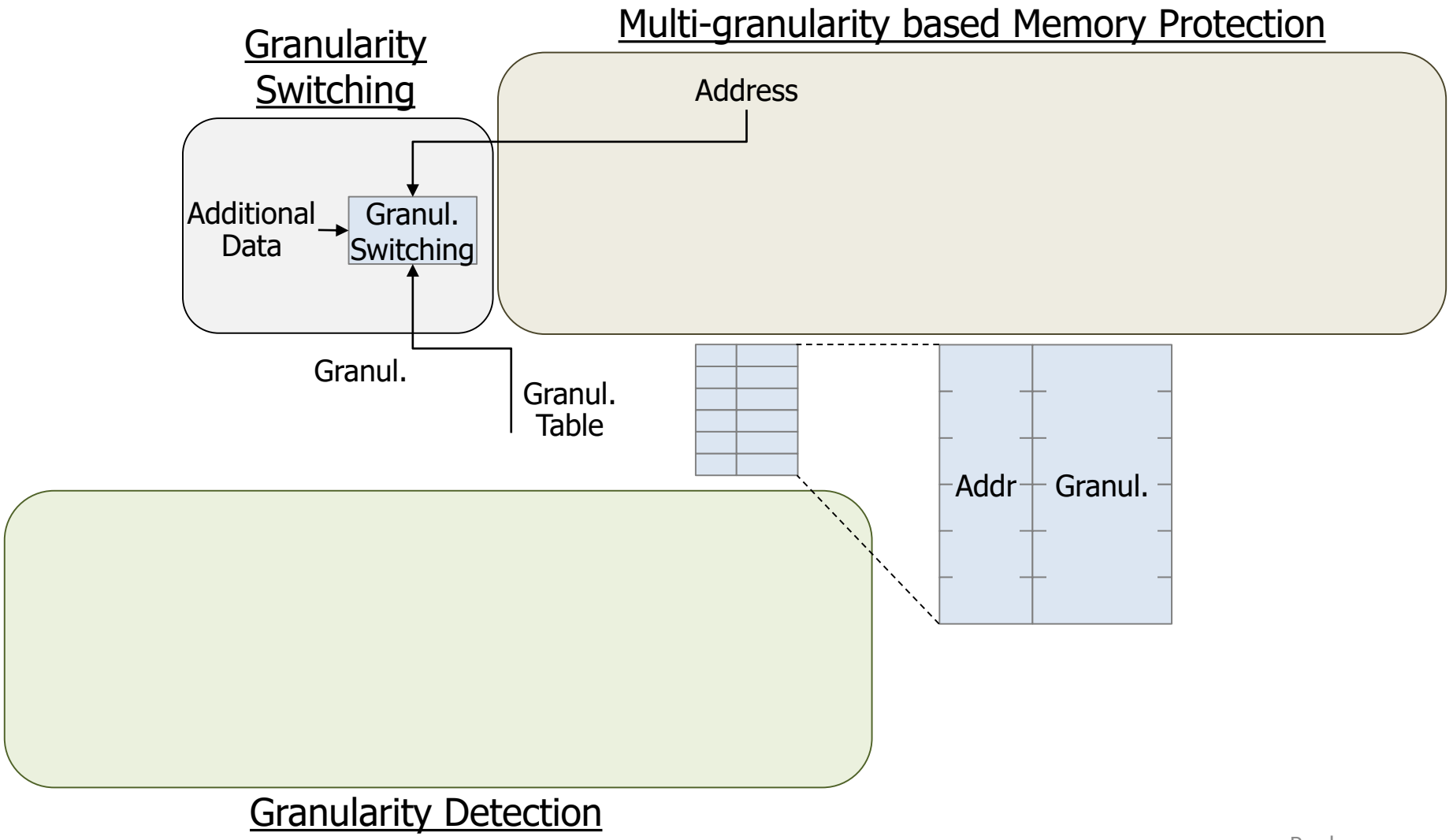

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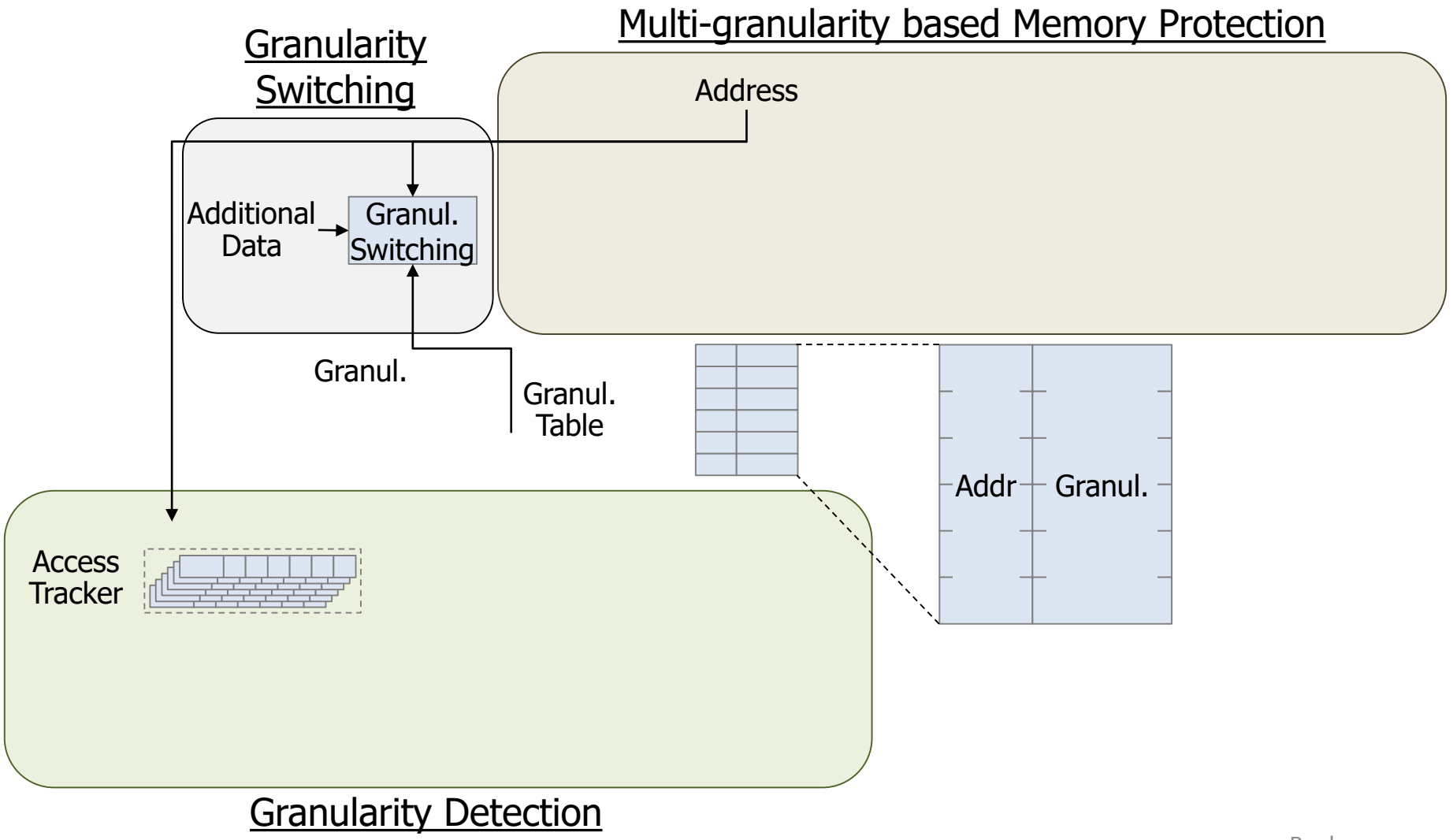

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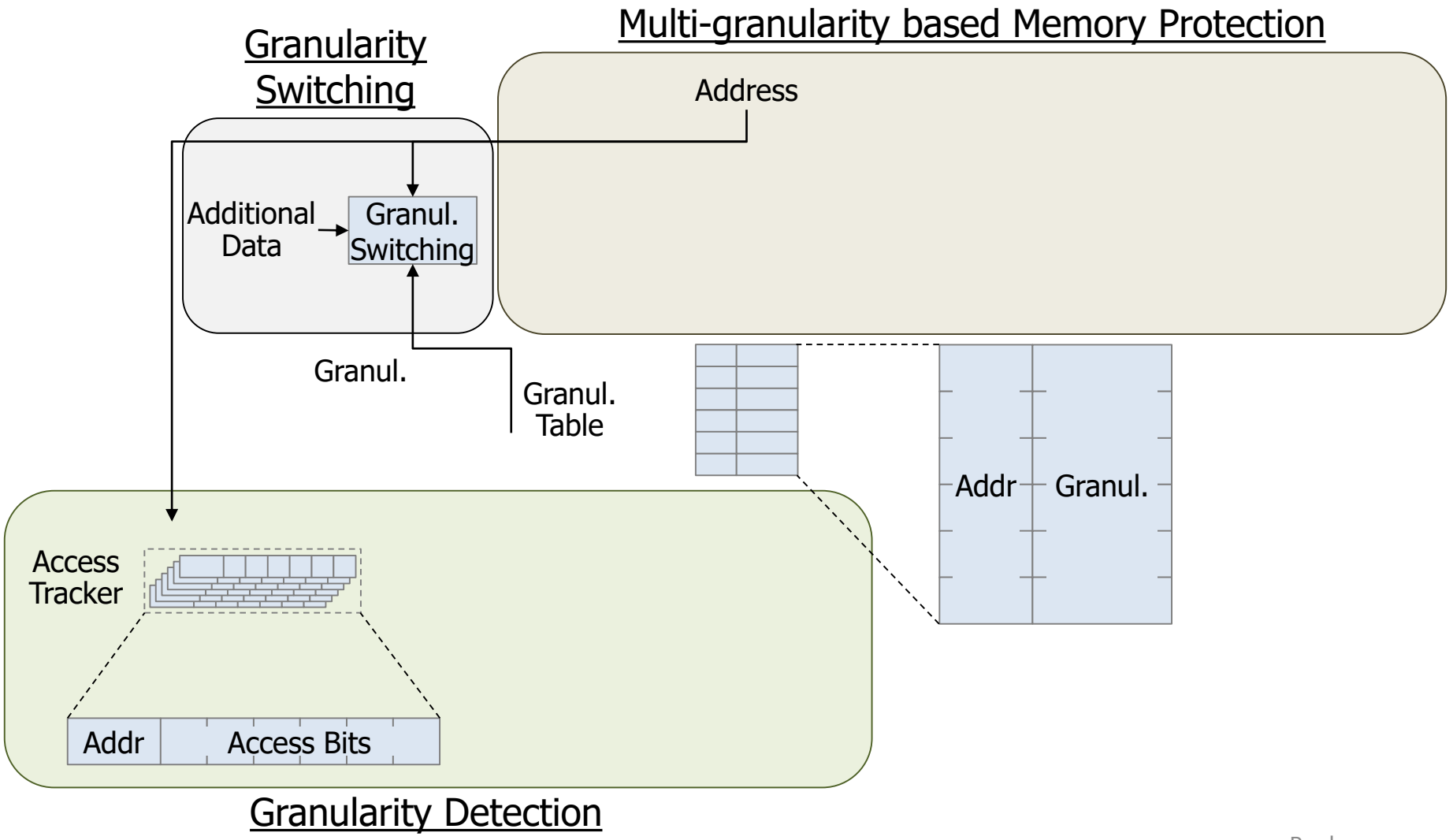

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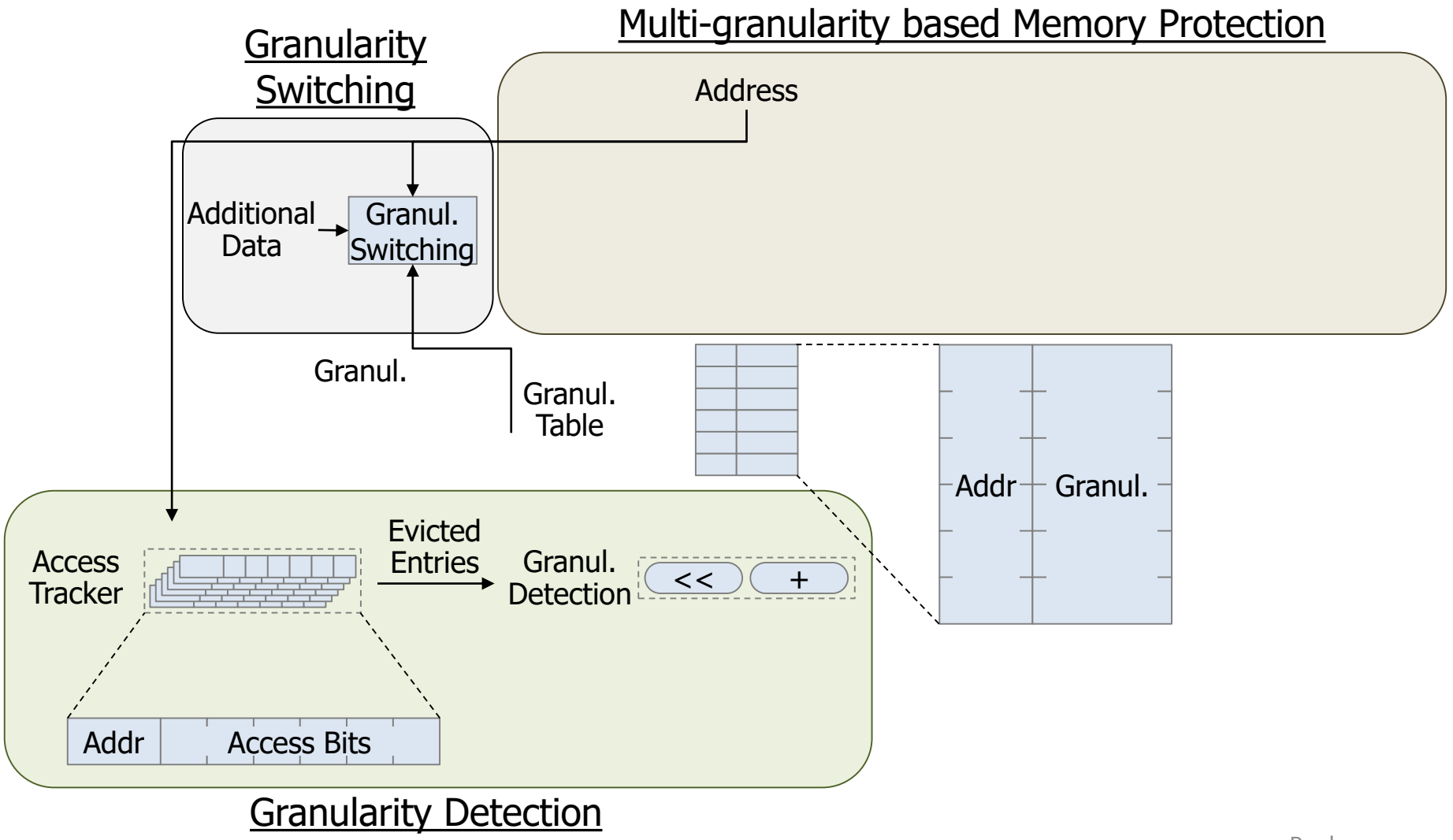

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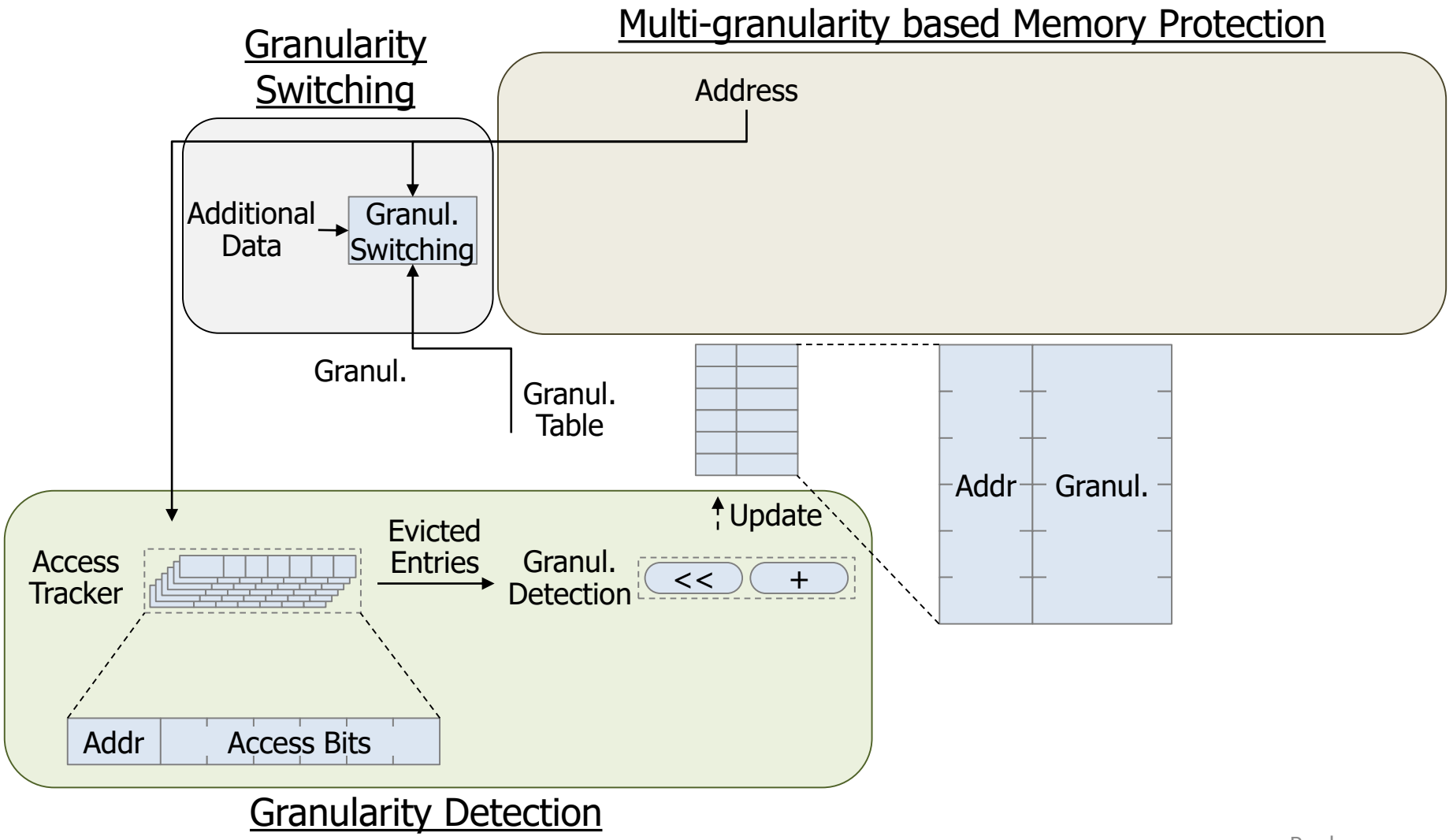

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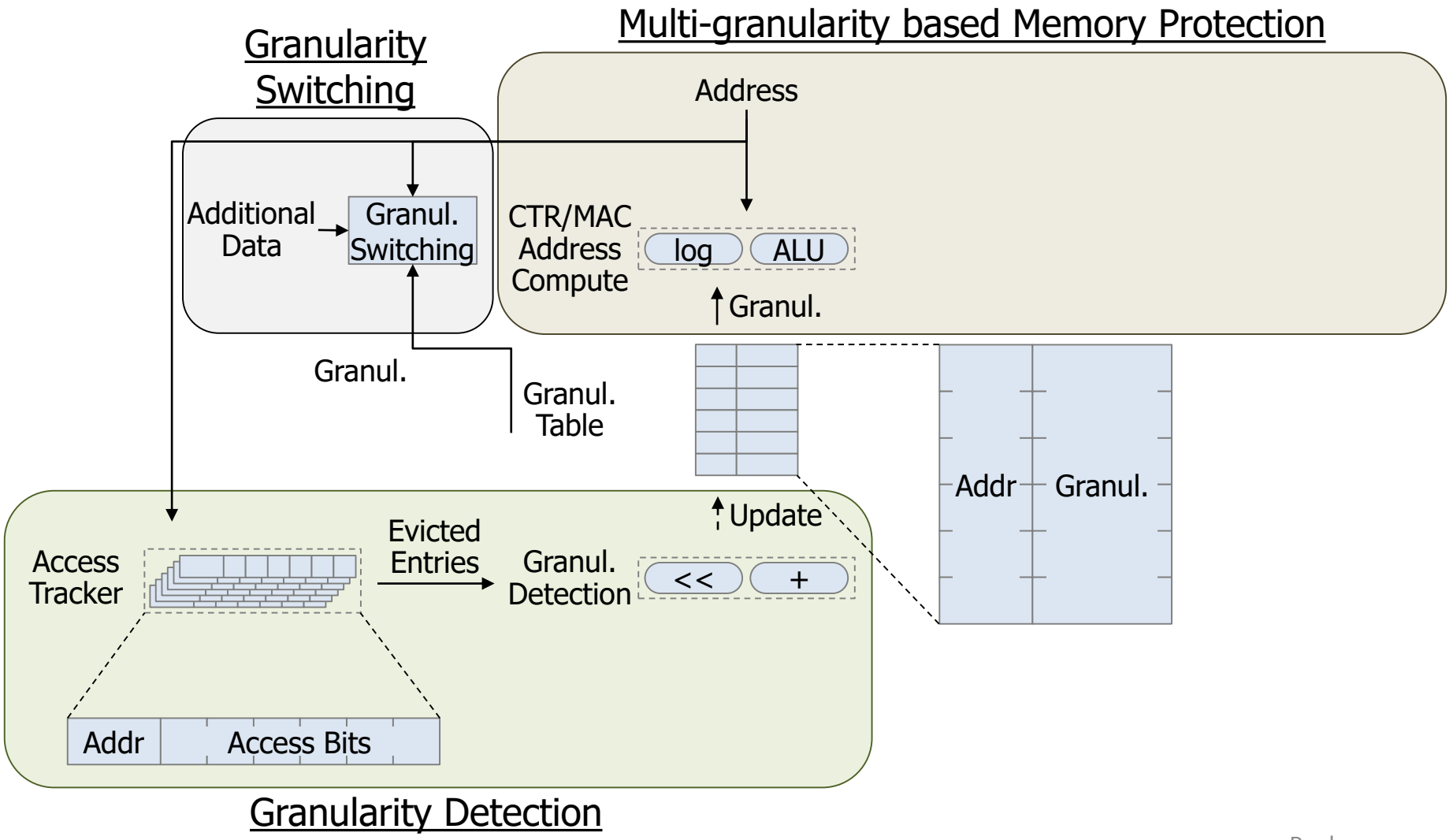

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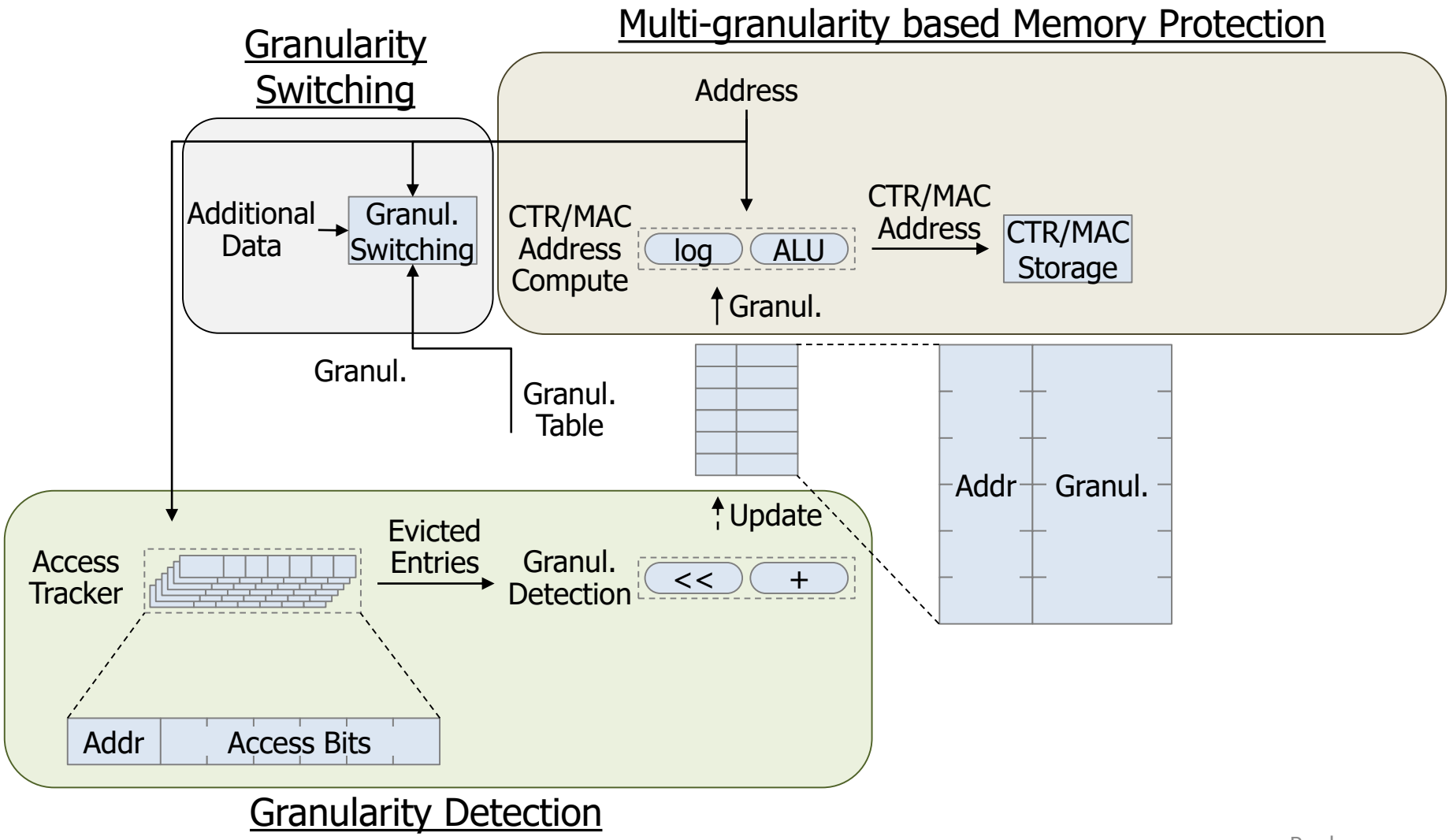

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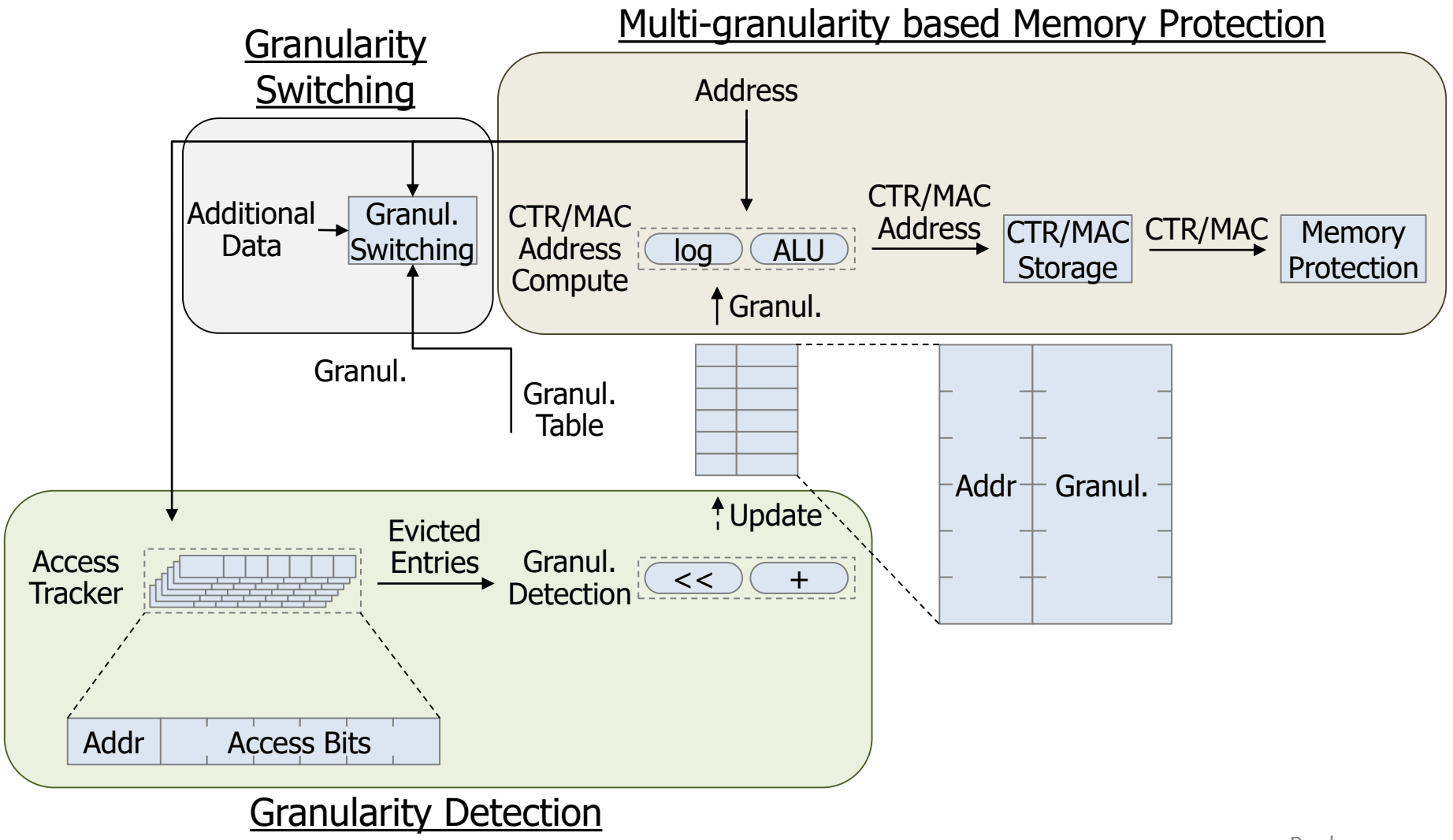

# Recent Memory Protection Studies

# Recent Memory Protection Studies

| Study | Target | Multi CTR | Int. Tree Opt. | Multi MAC | Dynamic Update | Target App. |
|---|---|---|---|---|---|---|
| *SoftVN* | CPU | O | X | X | X | ML-specific |
| *Common Counters* | GPU | Dual | X | X | X | General |
| *Adaptive* | GPU | X | X | Dual | O | General |
| *TNPU* | NPU | O | X | X | X | ML-specific |
| *Tunable Tree* | NPU | O | Sub Optimal | X | X | General |
| *MGX* | NPU | O | X | O | X | ML-specific |
| *GuardNN* | NPU | O | X | X | X | ML-specific |
| *TensorTEE* | CPU+NPU | O | X | O | O | ML-specific |
| **Ours** | **CPU+GPU +NPU** | **O** | **Optimal** | **O** | **O** | **General** |

# Prior Integrity Tree Optimization

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|---|---|---|---|---|---|---|
| *Bonsai Merkle Forests* | CPU | X | Sub Optimal | X | X | General |
| *PENGLAI* | GPU | X | Sub Optimal | X | X | General |
| *Migratable Merkle Tree* | GPU | X | Sub Optimal | X | X | General |
| *Data Enclave* | NPU | X | Sub Optimal | X | X | General |
| **Ours** | CPU+GPU +NPU | O | Optimal | O | O | General |

# Encryption & Integrity Validation using Coarse-grained MAC & Counter

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- Coarse-MAC & counter encryption, integrity validation

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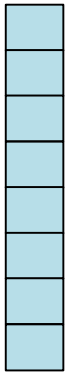
512B



$CTR_{course(1 \cdots 8)}$

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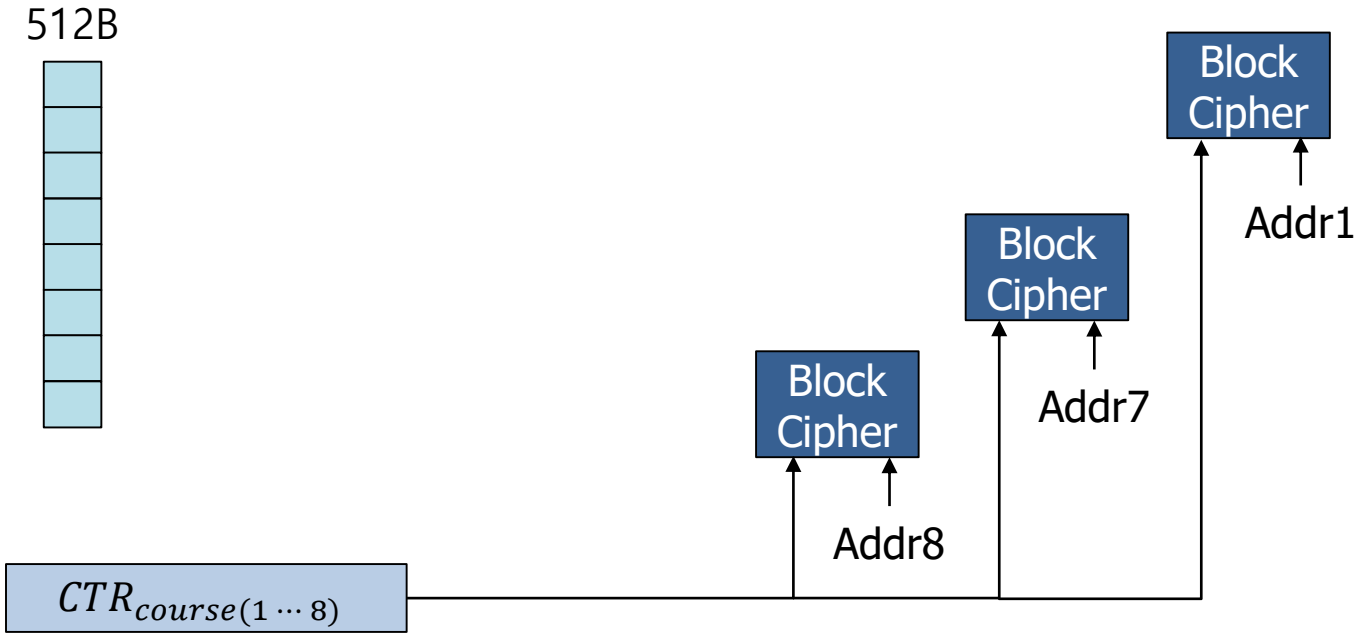

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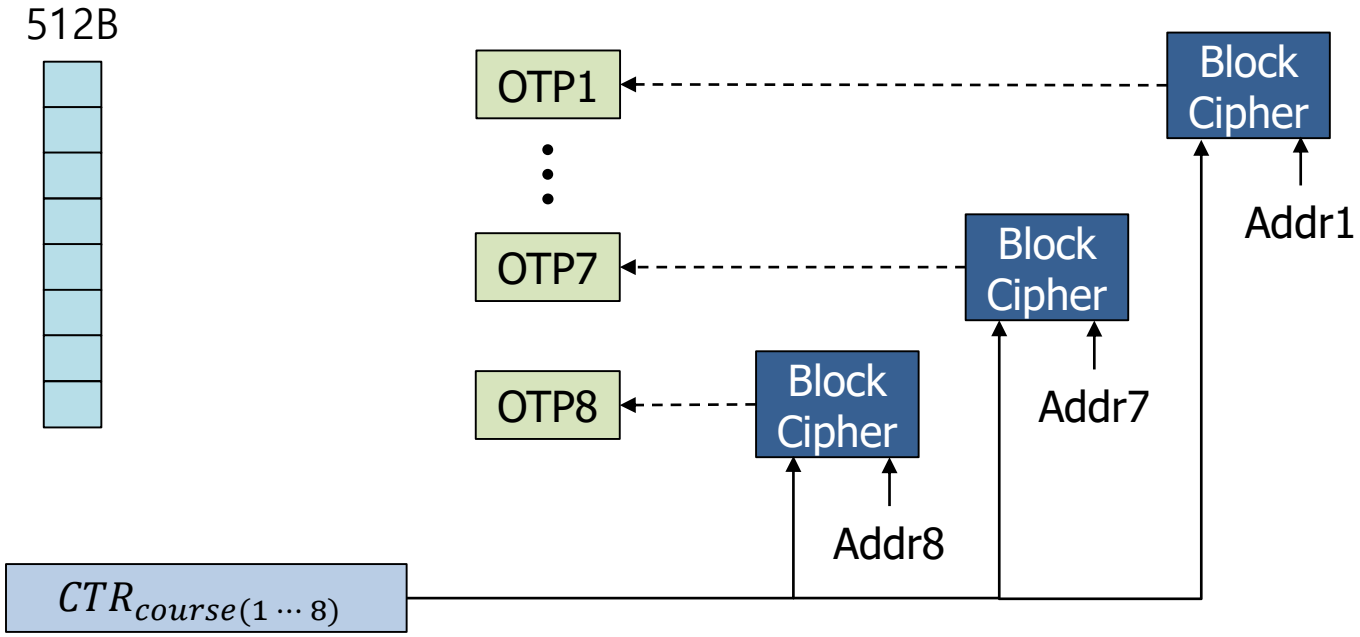

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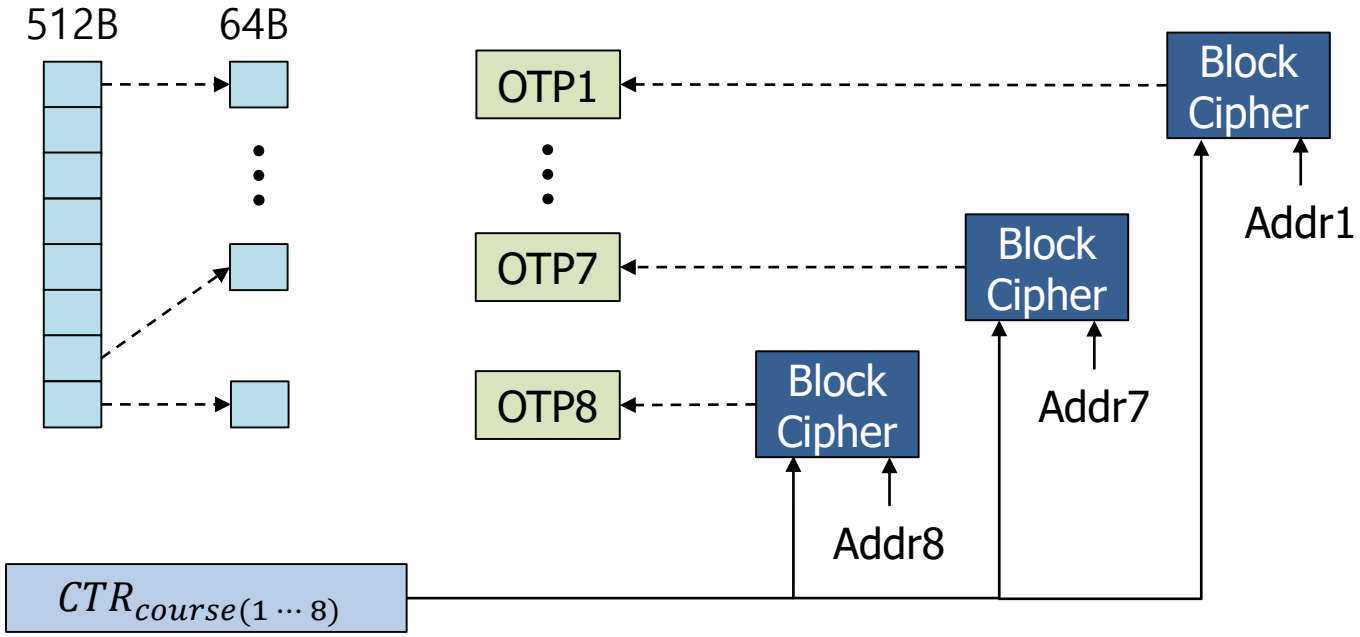

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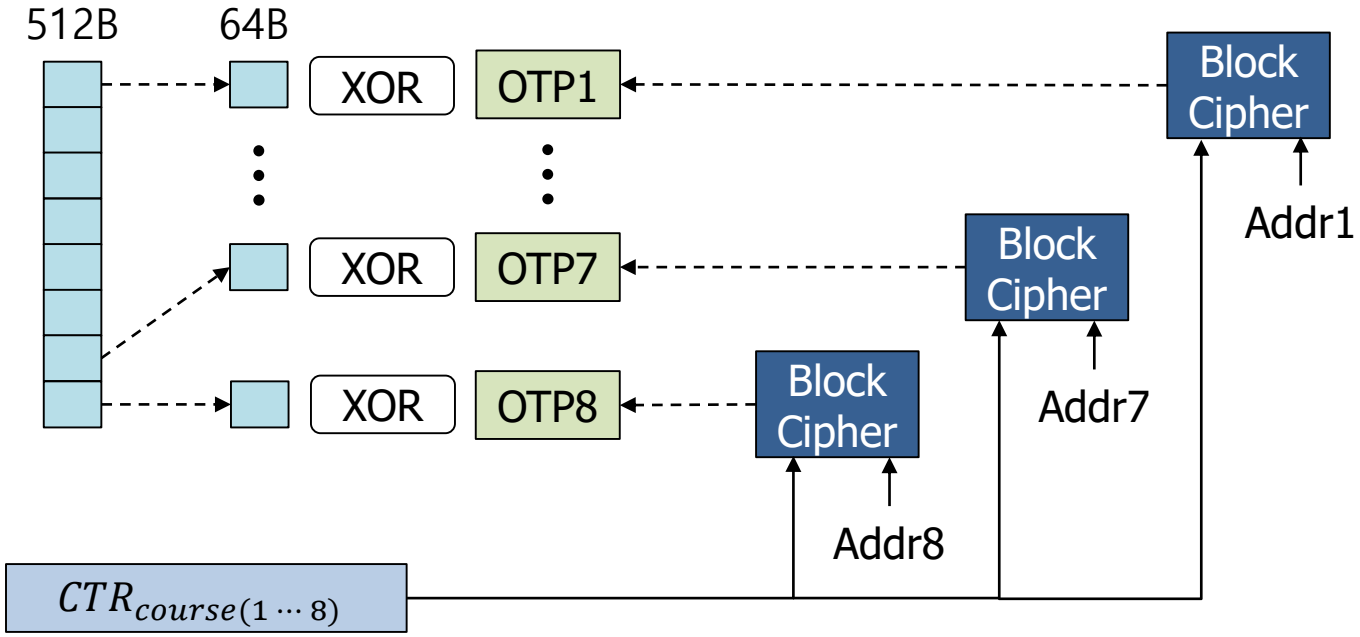

# Address of MAC & Counter

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- Chunk-level index computation

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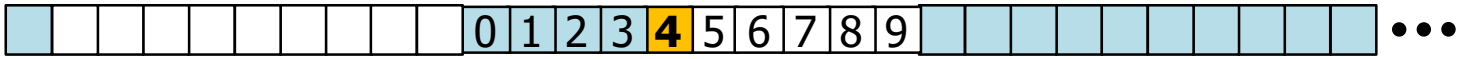

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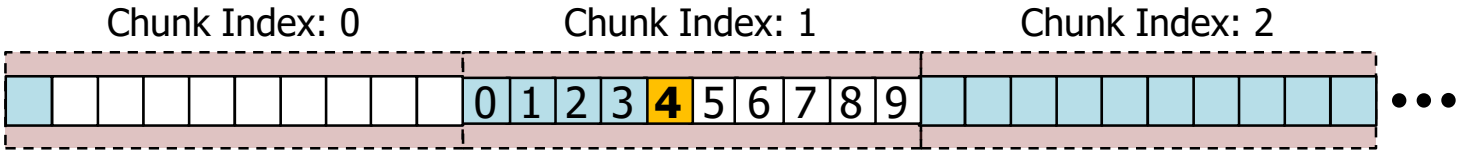

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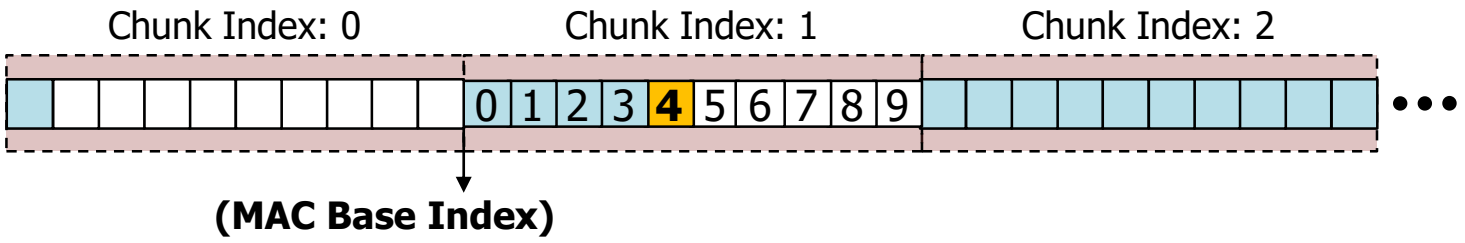

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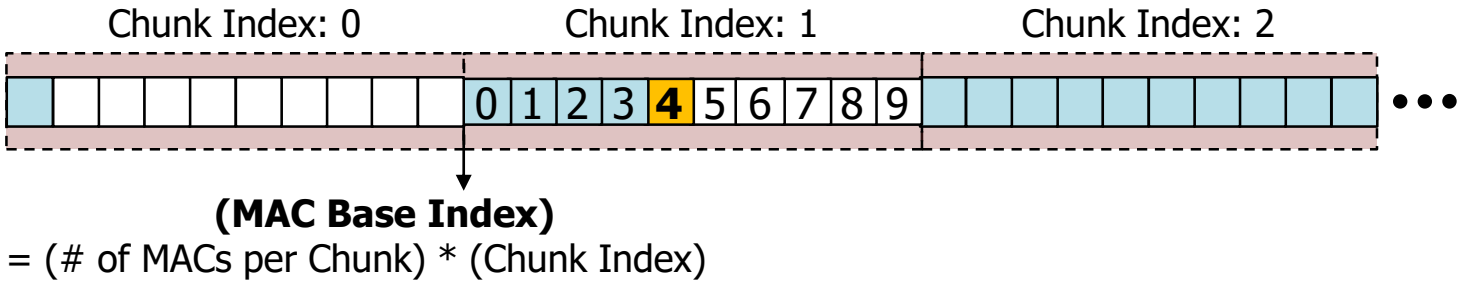

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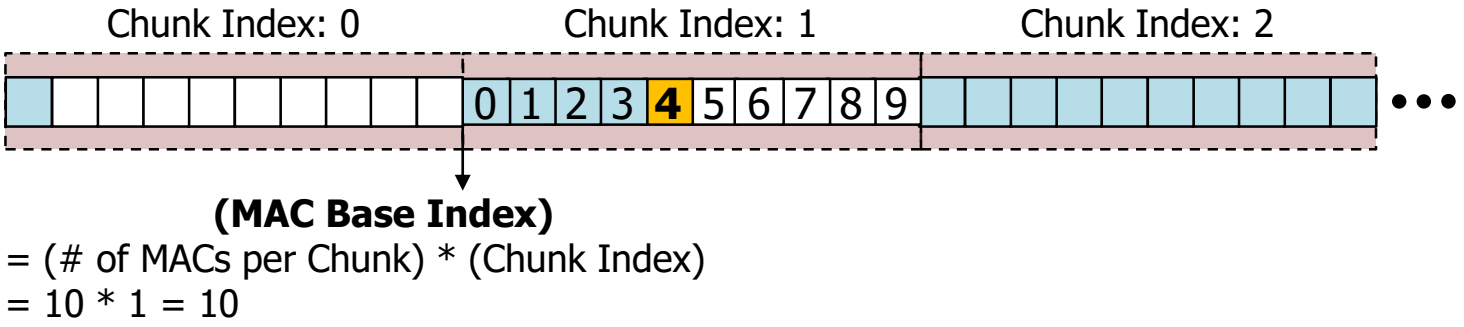

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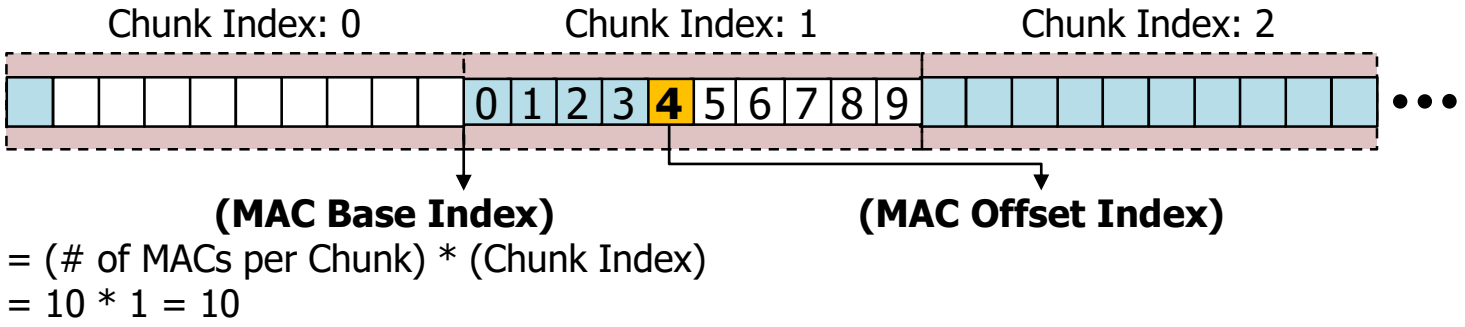

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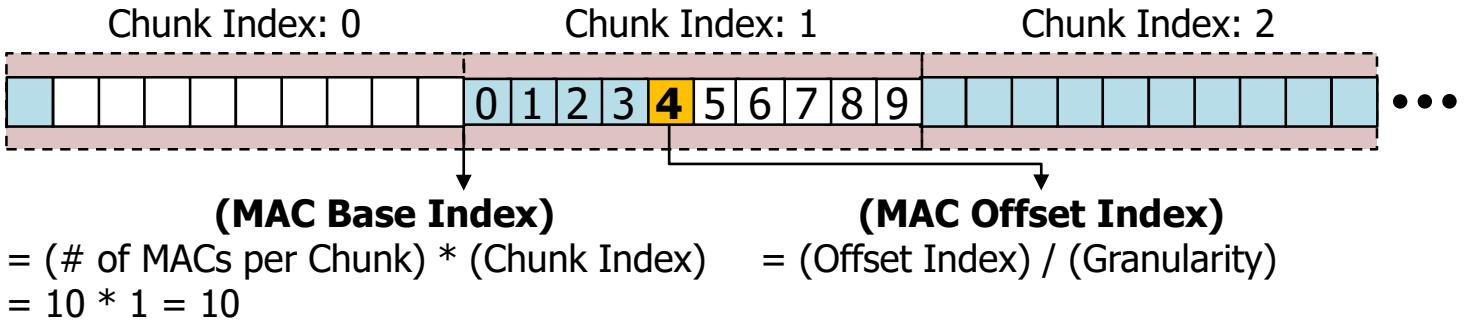

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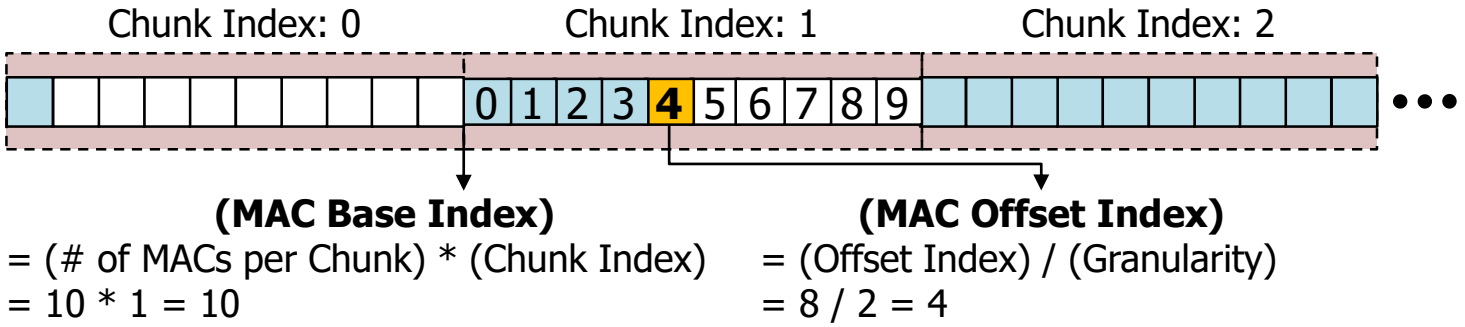

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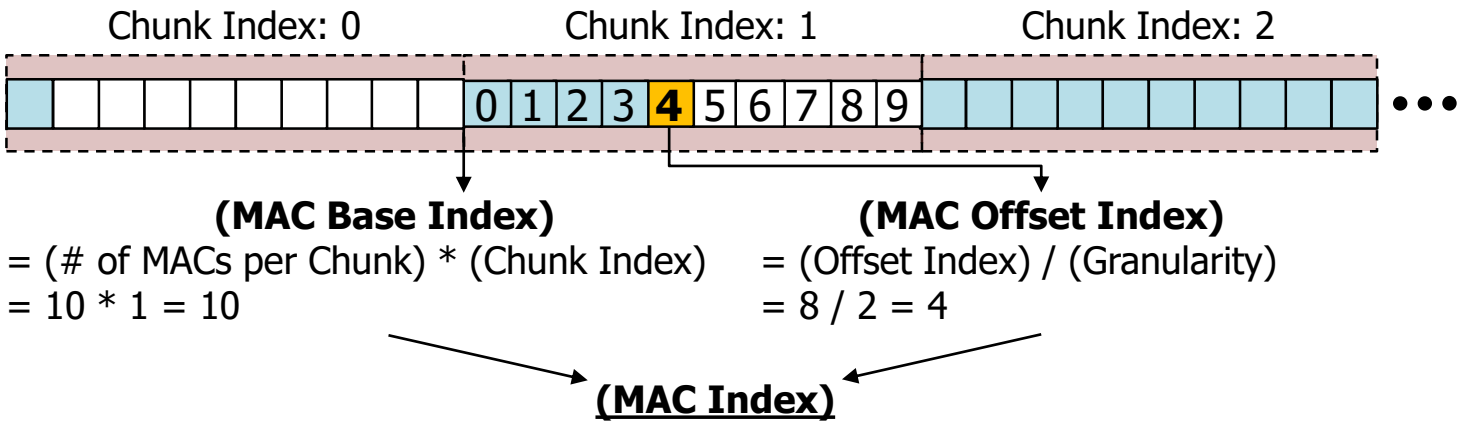

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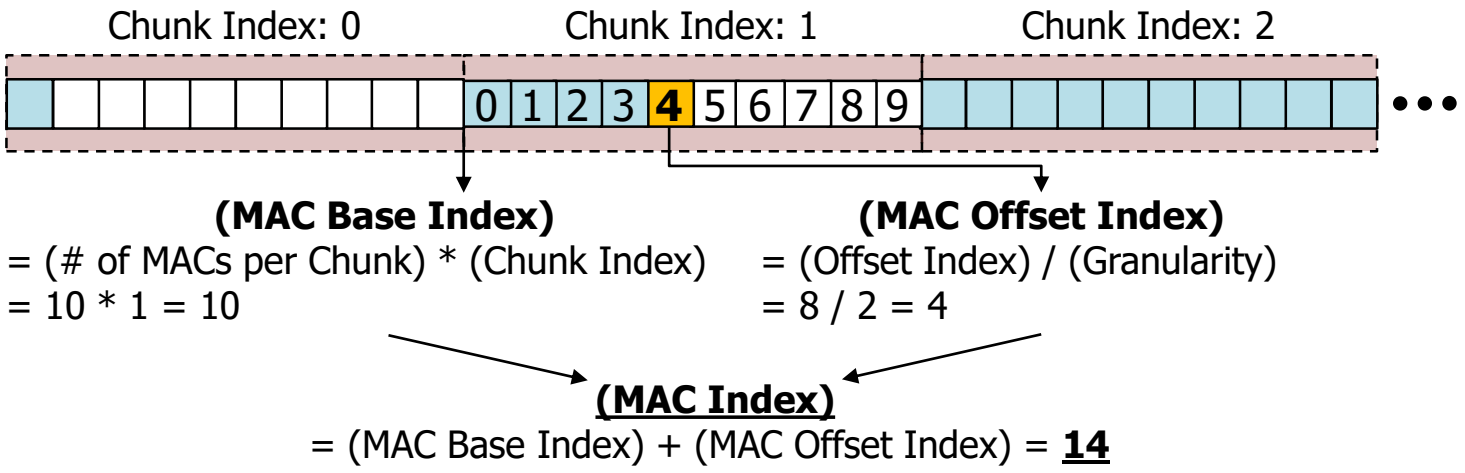

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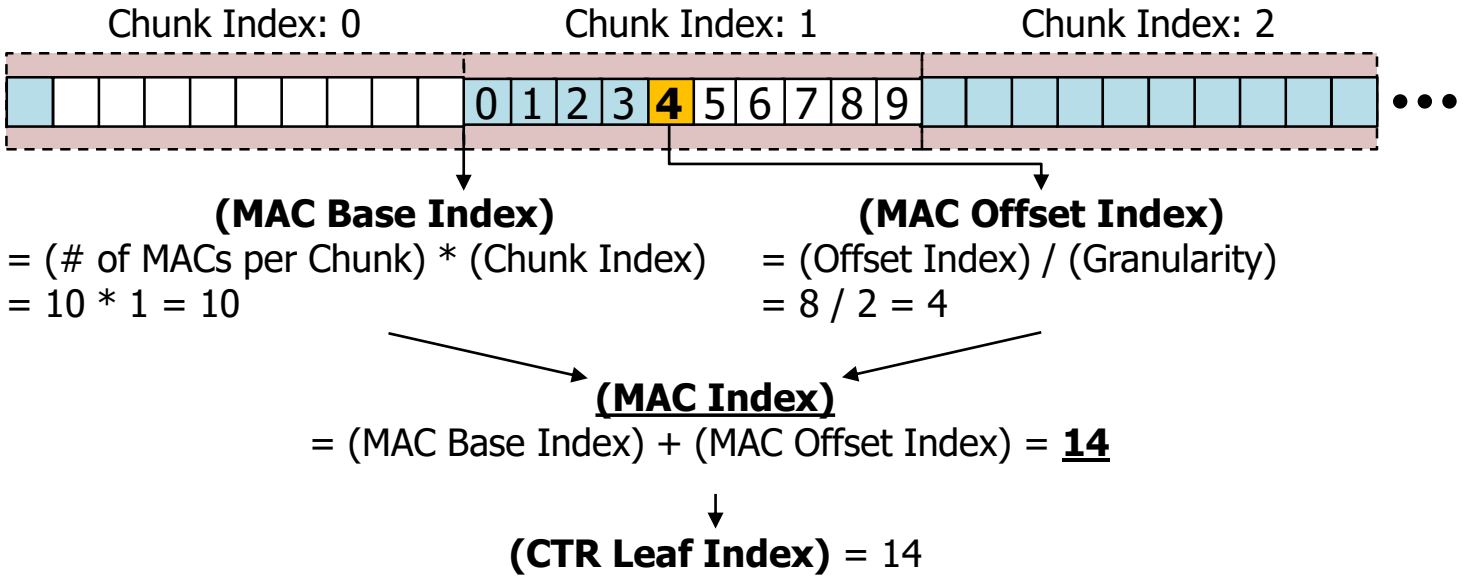

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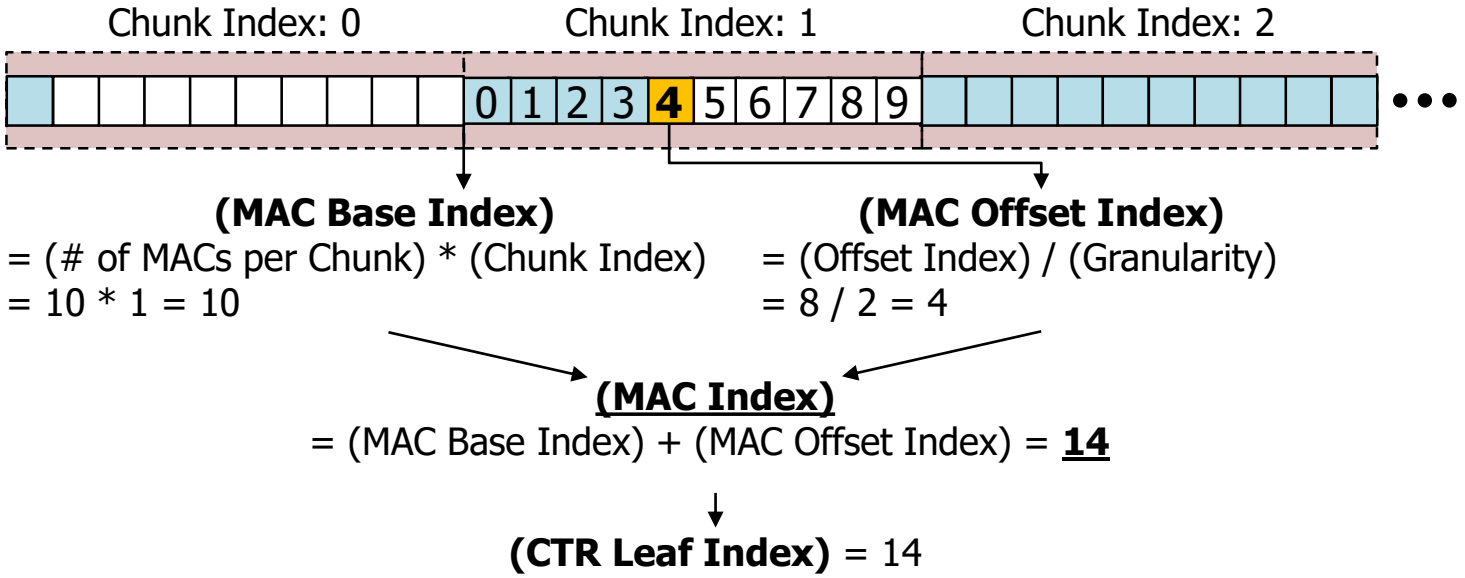


**(# of Parents)**

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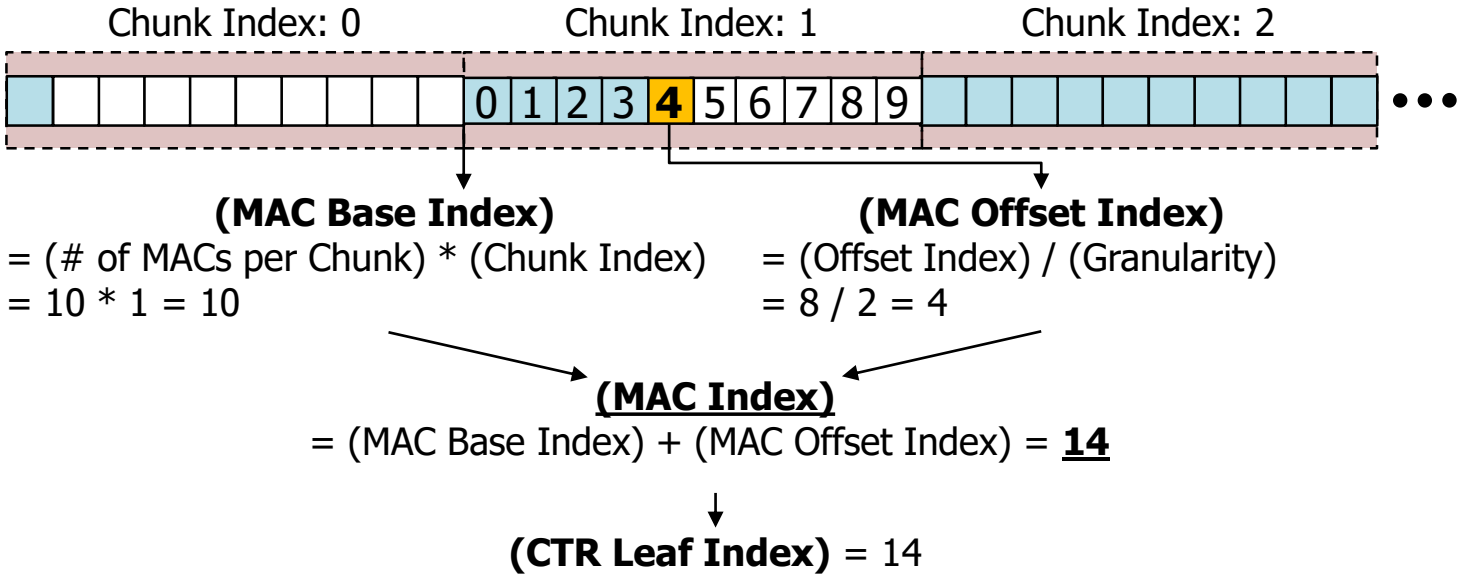


**(# of Parents)**
= sqrt{Arity}(Granularity)

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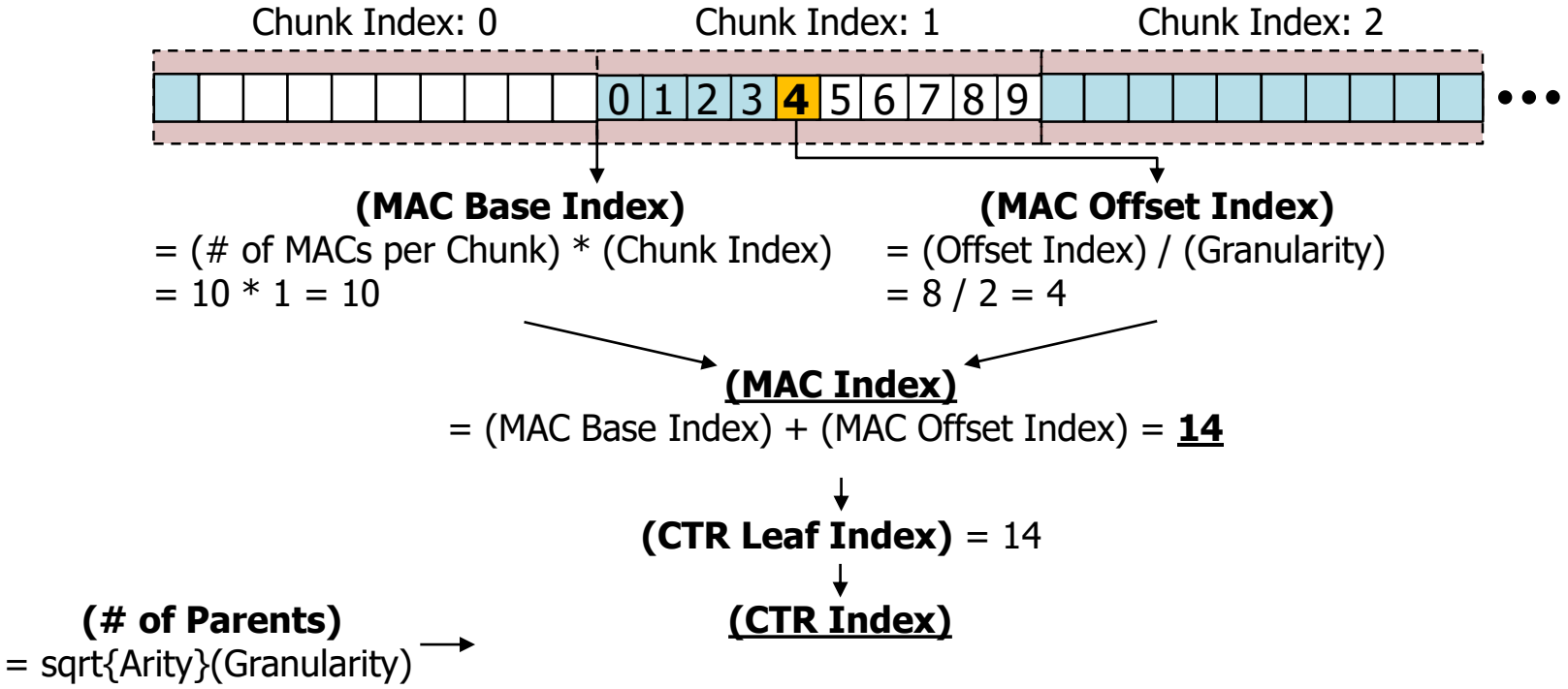

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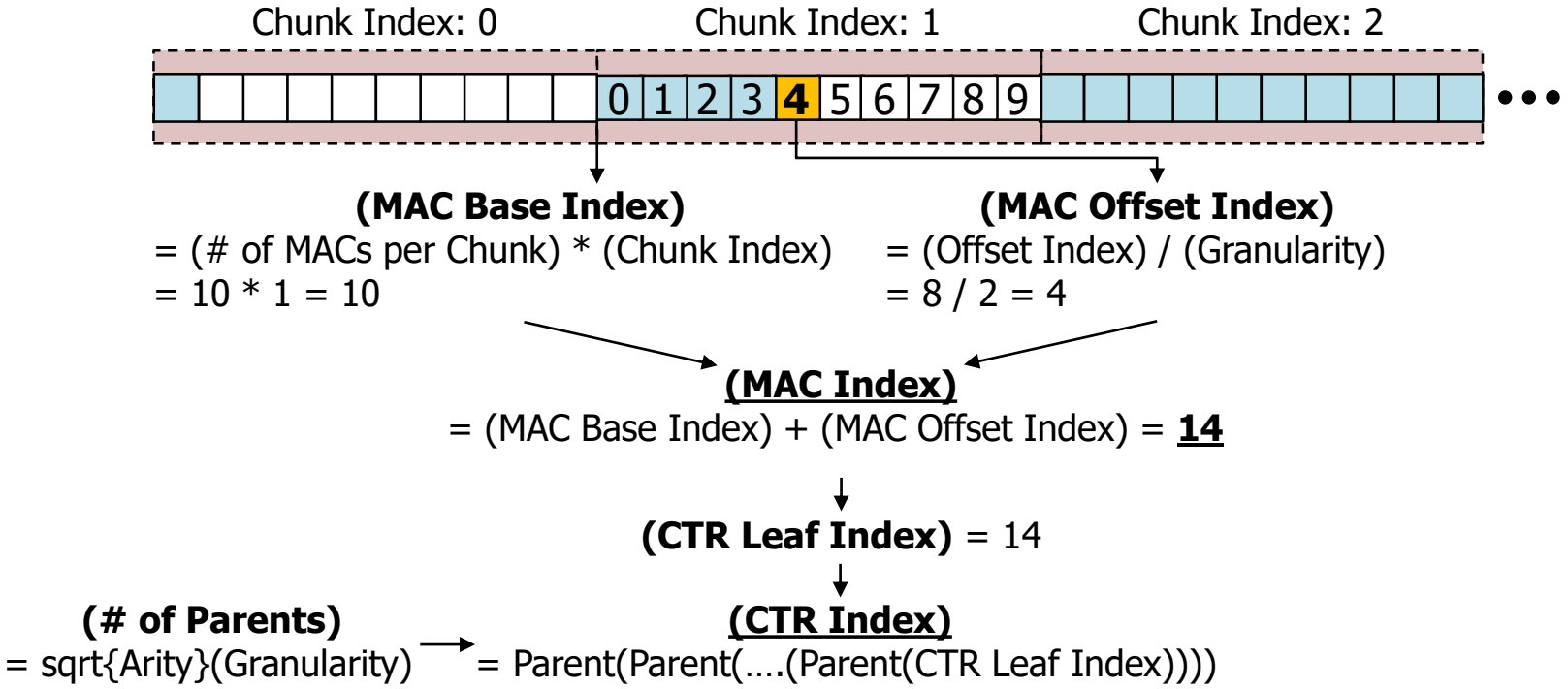

# Workload Analysis & Selected Scenarios

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- Workloads & Scenarios

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- Workloads & Scenarios
  - 14 workloads, 250 scenarios (all combinations)
  - Access pattern: Fine – ff – f – c – cc – Coarse | Diverse (d)
  - Traffic per cycles: Small (s) – Medium (m) – Large (l)

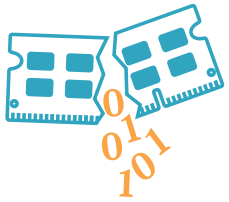
| | Workloads (access pattern-traffic per cycles) |
|---|---|
| CPU | bw (ff-s), gcc (ff-s), mcf (ff-m), xal (f-m), ray (ff-s) |
| GPU | syr2k (ff-m), pr (f-m), sten (c-l), mm (cc-m), floyd (d-s), |
| NPU | ncf (c-s), dlrm (c-s), sfrnn (c-l), alex (cc-m) |

| ID | (CPU, GPU, NPU1, NPU2) |
|---|---|
| ***ff*** | (bw, syr2k, ncf, dlrm), (mcf, syr2k, sfrnn, dlrm), (gcc, floyd, sfrnn, ncf) |
| ***f*** | (xal, pr, sfrnn, ncf), (xal, pr, ncf, ncf) |
| ***c*** | (gcc, sten, alex, dlrm), (bw, sten, ncf, ncf), (mcf, sten, sfrnn, sfrnn) |
| ***cc*** | (xal, mm, alex, dlrm), (ray, mm, alex, alex), (ray, Floyd, alex, alex) |

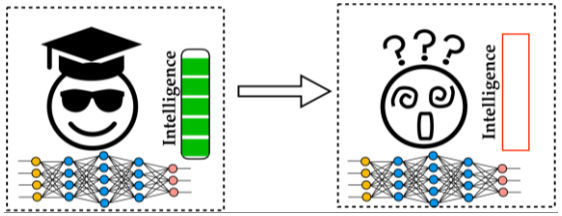
# Rowhammer Attacks

```
1 code1a:
2   mov (X), %eax
3   mov (Y), %ebx
4   clflush (X)
5   clflush (Y)
6   mfence
7   jmp code1a
```

Bit-flip[1]




RamBleed[2]




DeepHammer[3]


[1] Flipping Bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors (ISCA 2014)
[2] RAMBleed: Reading Bits in Memory Without Accessing Them (S&P 2020)
[3] DeepHammer: Depleting the Intelligence of Deep Neural Networks through Targeted Chain of Bit Flips (USENIX Security 2020)

# More Design Descriptions in Our Paper

- Lazy-switching analysis
- Cacheline fragmentation issue
- CTR/MAC addressing for multi-granularity
- Coarse-grained memory protection engine using parallel counter sharing and nested MAC hasing
- Misprediction handler
- Efficient granularity representation
- Hardware overhead
- Comparison to prior subtree optimization schemes

# More Results in Our Paper

- The ratio of stream chunks
- Performance analysis of selected scenarios
- End-to-end performance
- Drawbacks of the per-device (static) granularity
- Performance comparison with dual-granularity
- Switching overhead measurement
- Security cache hit ratio improvement
- Hardware overhead

# Temp Slide

# Research Objective

Constructs a **general** and efficient memory protection scheme for heterogeneous processors

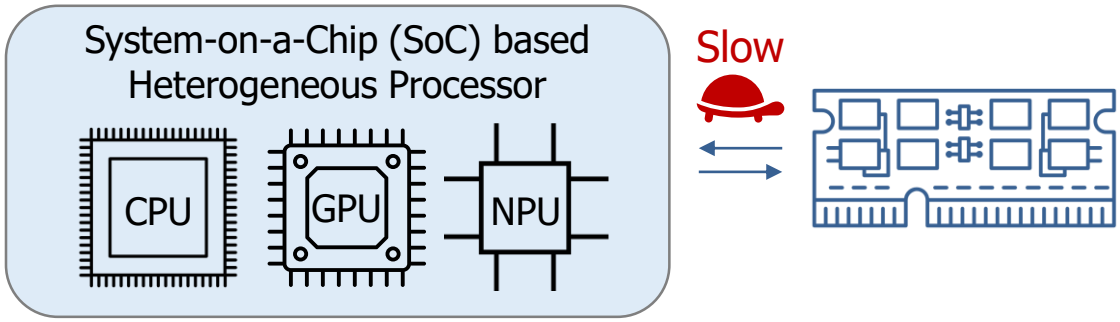
Temp

# Research Objective

Constructs a **general** and efficient memory protection scheme for heterogeneous processors

- Challenge 1: Heterogeneous processors have **diverse access pattern**

**Conventional Memory Protection: High Overhead**

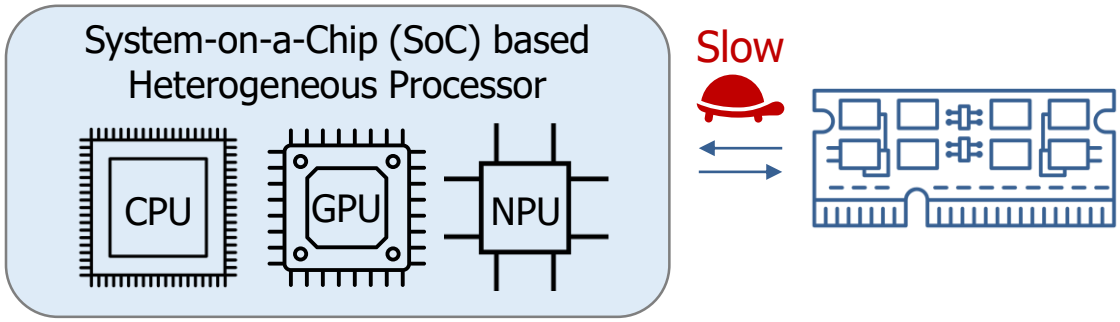


# Research Objective

Constructs a **general** and efficient memory protection scheme for heterogeneous processors

- Challenge 1: Heterogeneous processors have **diverse access pattern**
- Challenge 2: Each prior protection **only for a specific access pattern**

**Conventional Memory Protection: High Overhead**



# Research Objective

Constructs a **general** and efficient memory protection scheme for heterogeneous processors

- Challenge 1: Heterogeneous processors have **diverse access pattern**
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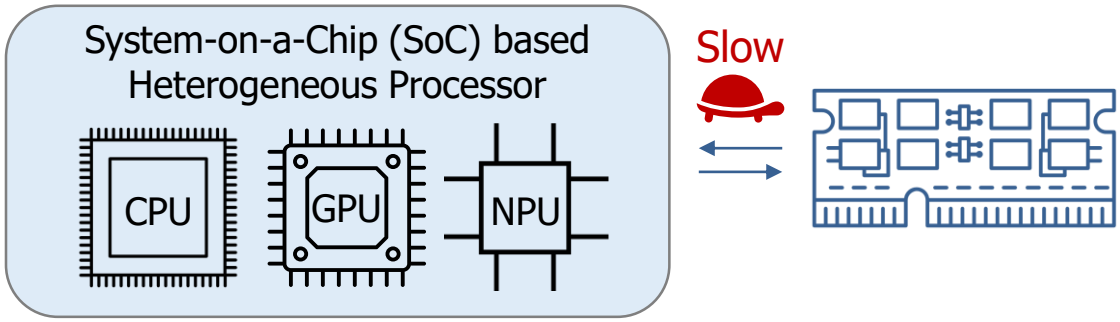


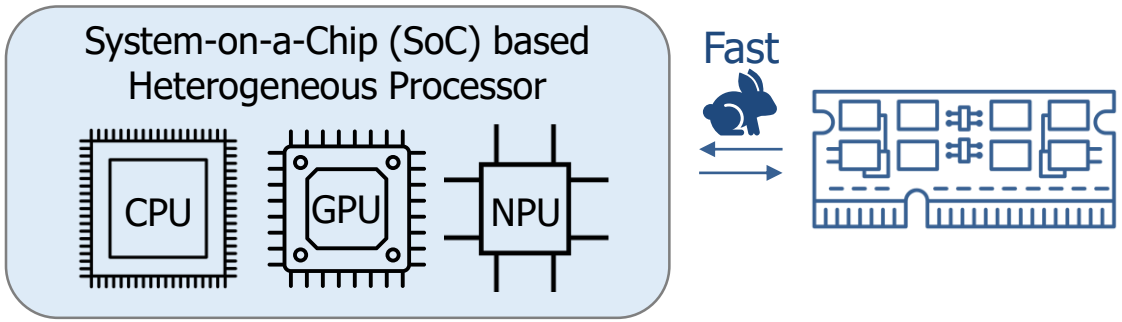
# Research Objective

Constructs a **general** and efficient memory protection scheme for heterogeneous processors

- Challenge 1: Heterogeneous processors have **diverse access pattern**
- Challenge 2: Each prior protection **only for a specific access pattern**
  - For example, GPU coarse-grained pattern, NPU software-detected pattern

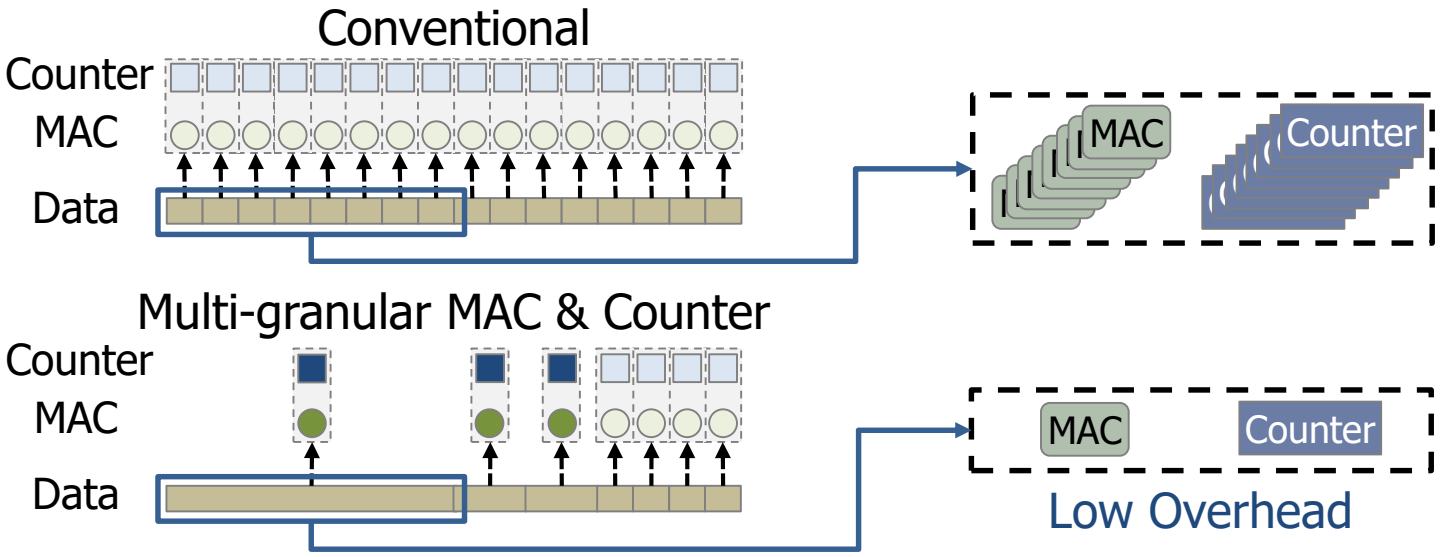
→ We **unified** prior studies with our novel multi-granular tree

**Our Unified Memory Protection Scheme**



# Multi-granular MAC and Counter

- Multi-granular MAC and counter
  - Multi-granular MAC and counter fetches **small # of MACs and counters** for coarse-grained access




**Multi-granularity can reduce memory protection overhead**
**However, how maintain a counter integrity tree?**

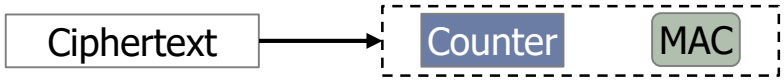
# Prior Memory Protection Schemes

# Prior Memory Protection Schemes

**Counter-mode Protection**

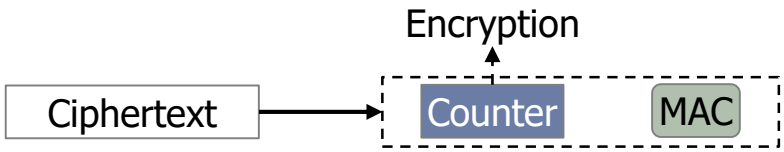
# Prior Memory Protection Schemes

**Counter-mode Protection**



# Prior Memory Protection Schemes

**Counter-mode Protection**



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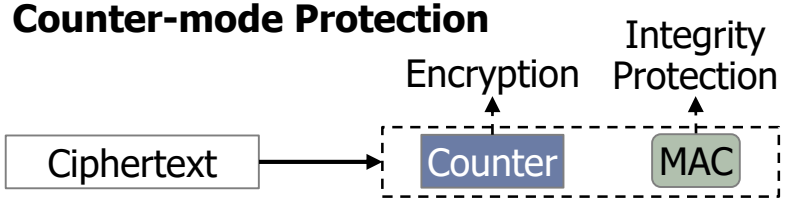

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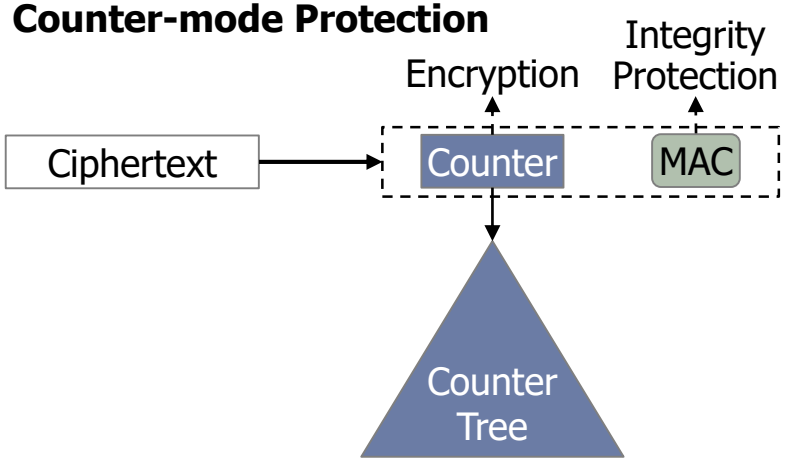

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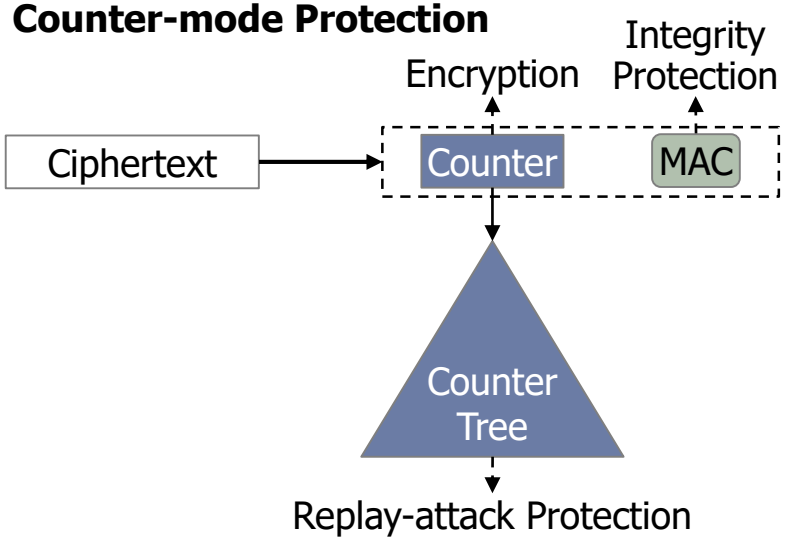

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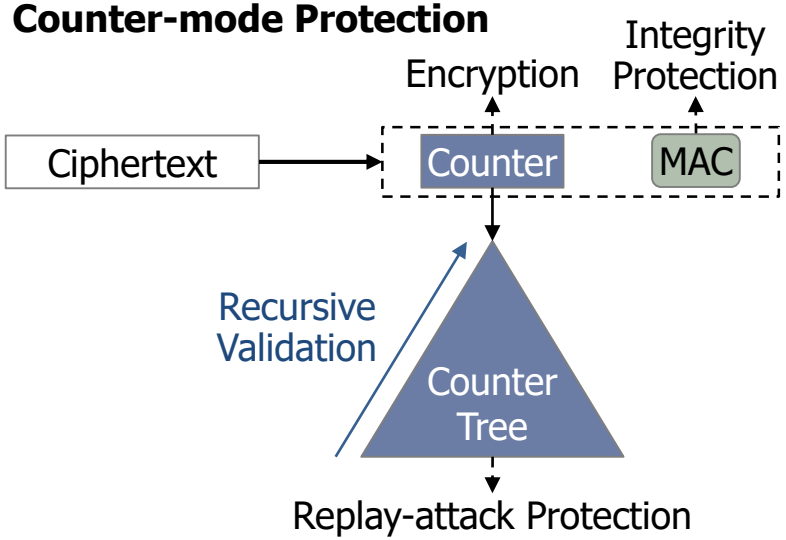

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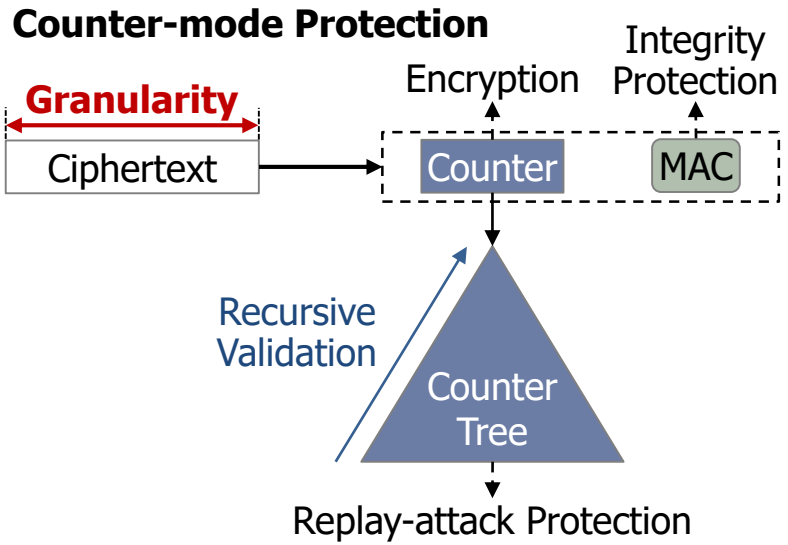

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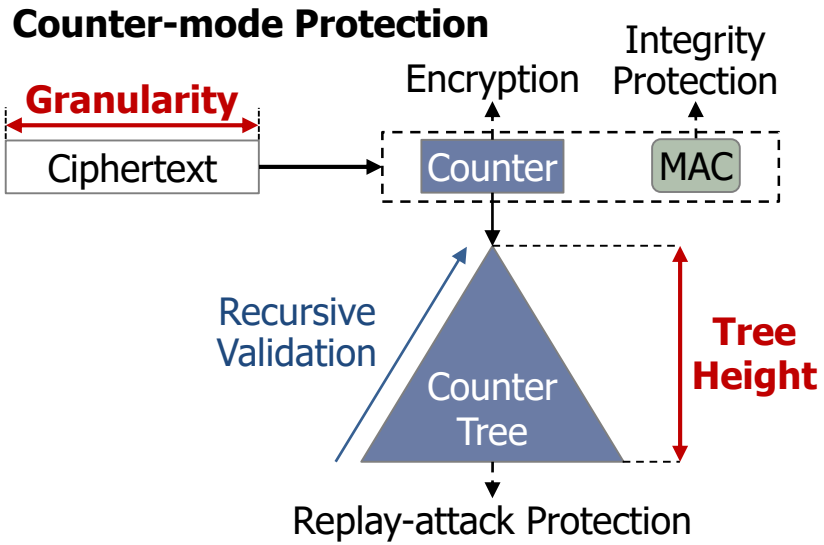

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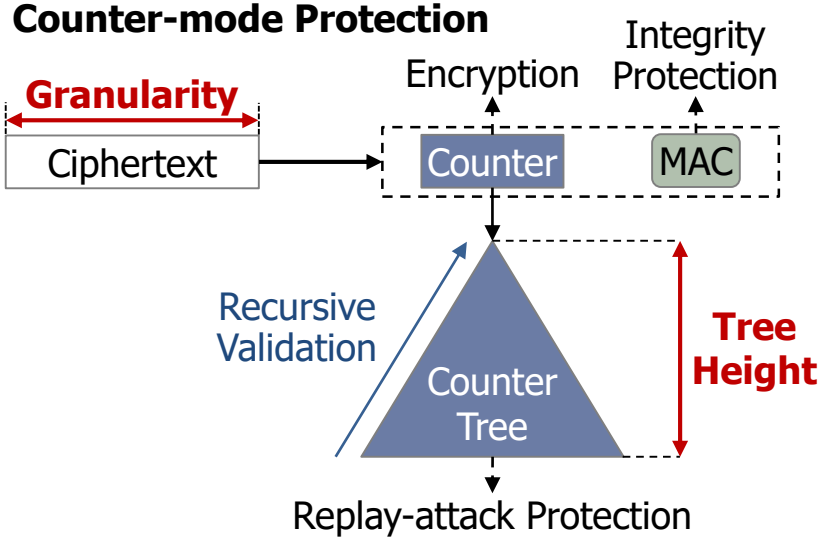
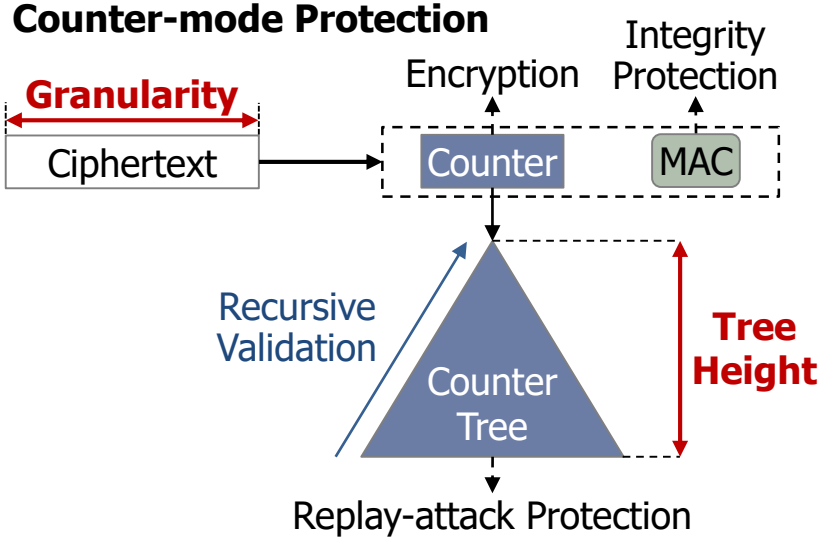



**Conventional 64B-granular Protection**

# Prior Memory Protection Schemes

**Counter-mode Protection**

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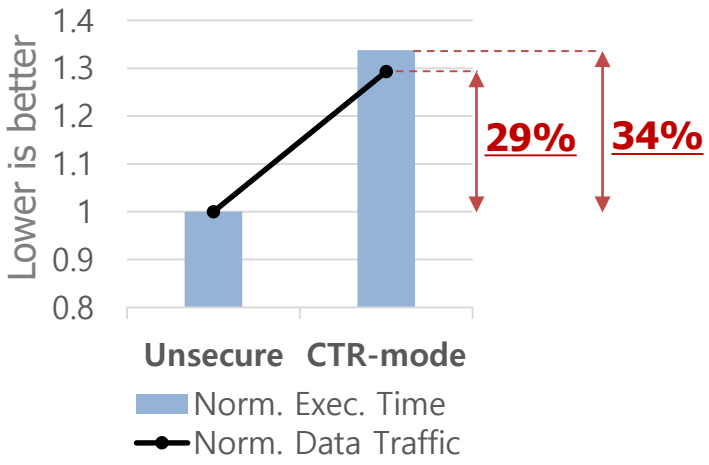

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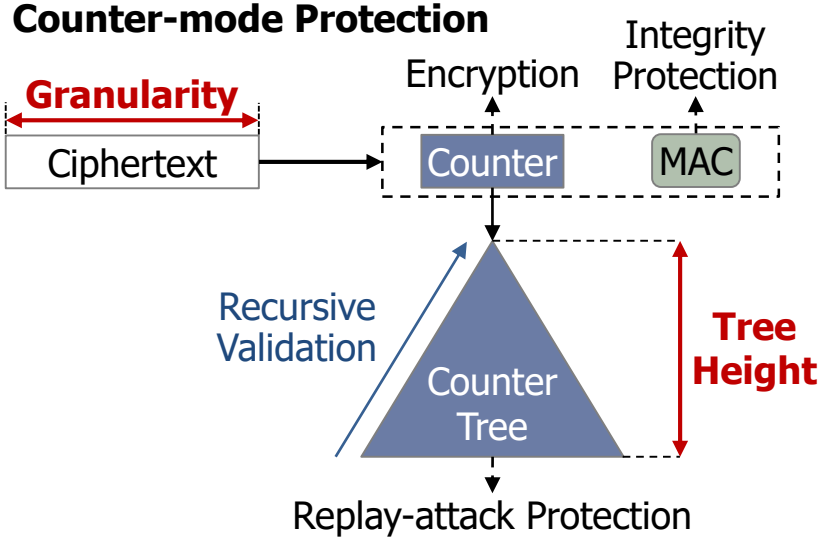


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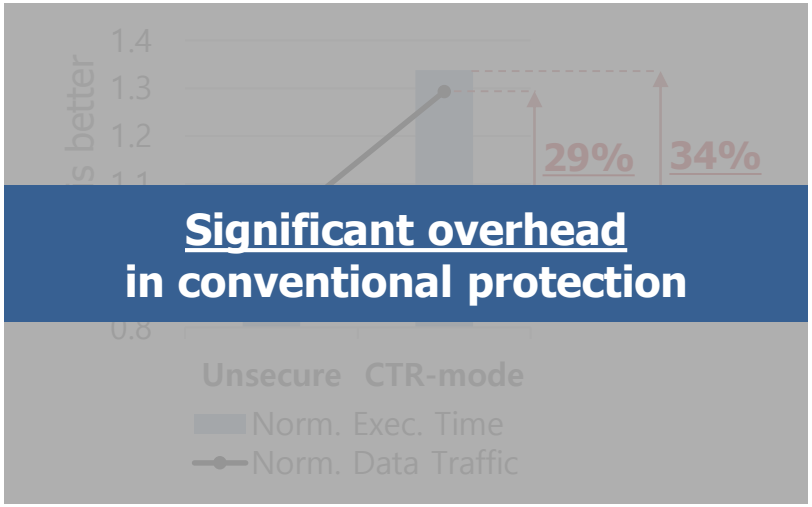

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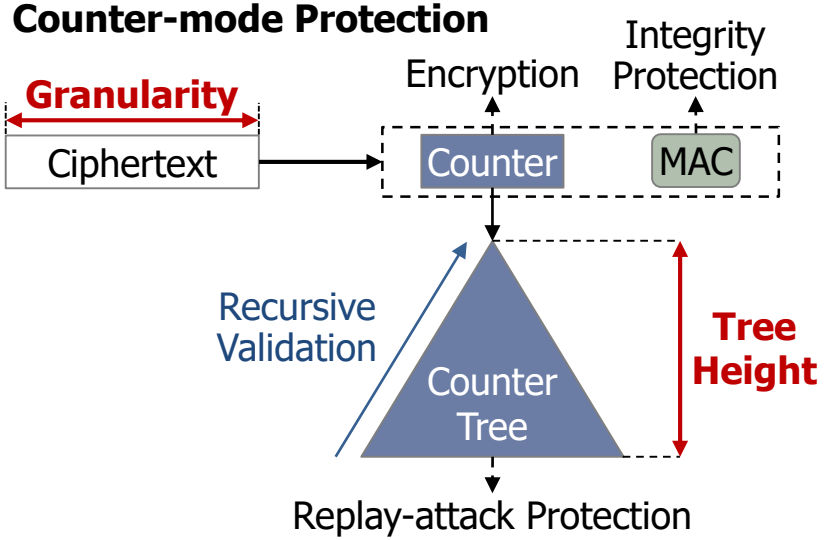


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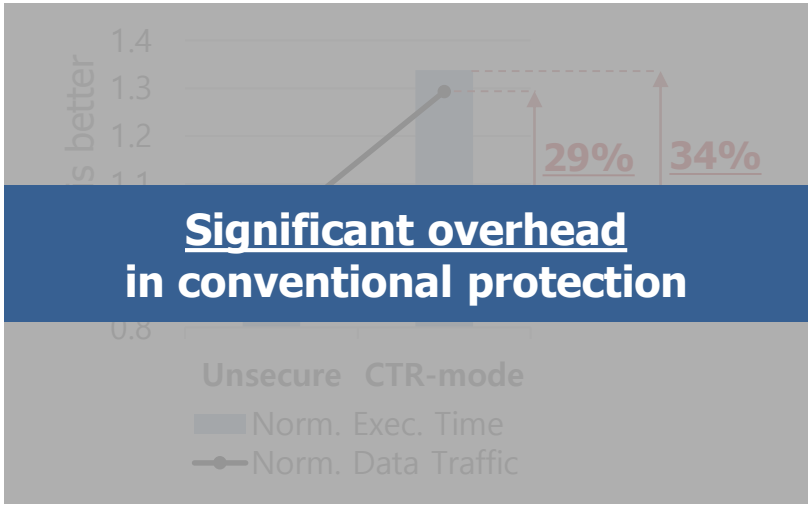
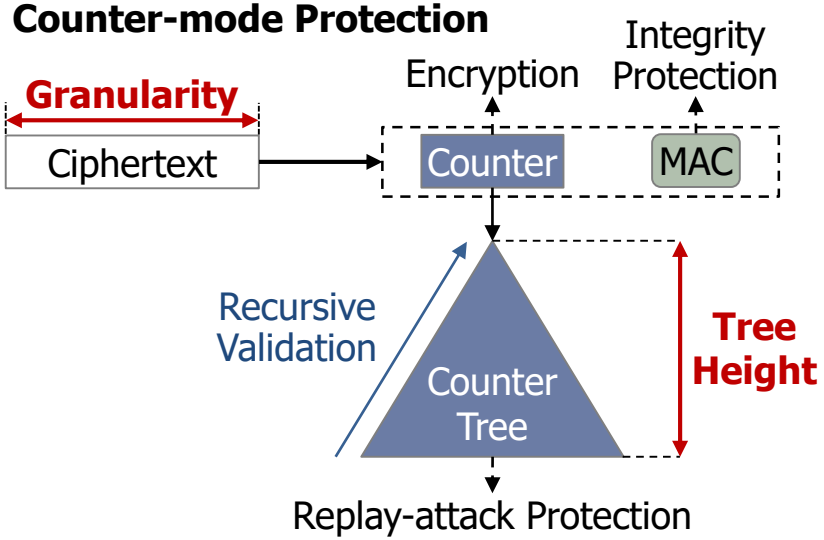



**Prior Domain-specific Memory Protection**

# Prior Memory Protection Schemes

**Counter-mode Protection**

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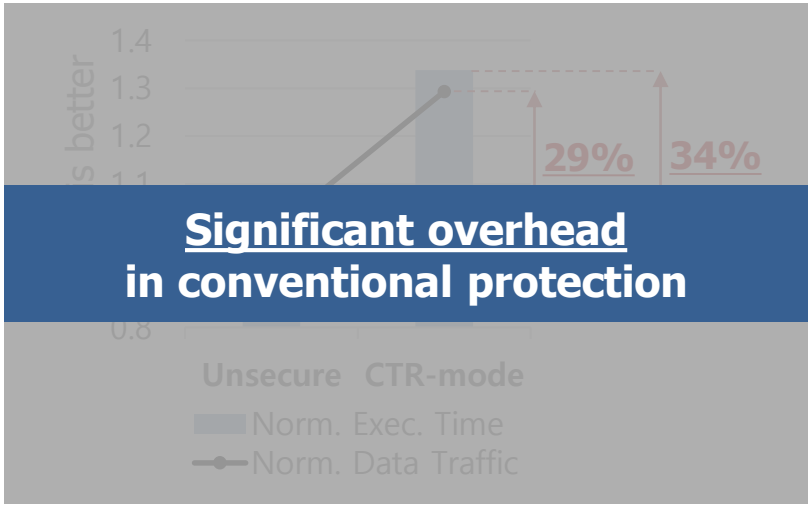


**Prior Domain-specific Memory Protection**

1. Common Counters [1]

[1] Common Counters: Compressed Encryption Counters for Secure GPU Memory (HPCA 2021)

# Prior Memory Protection Schemes

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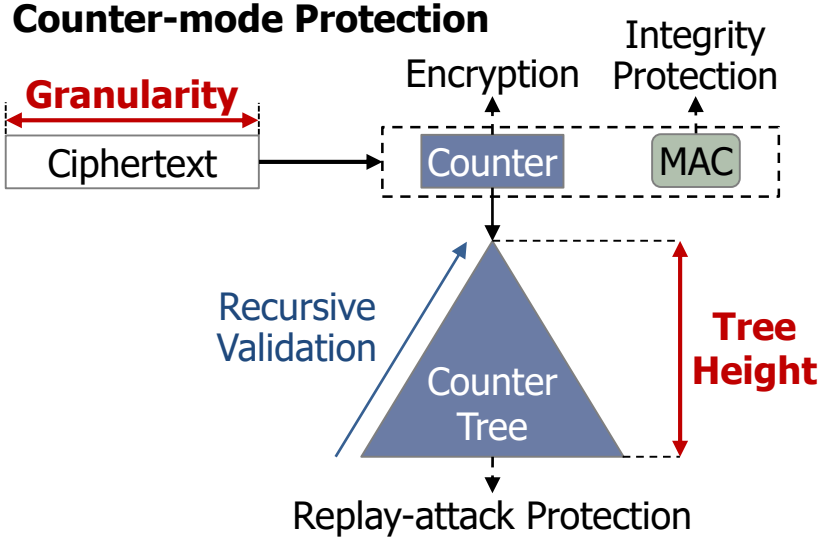
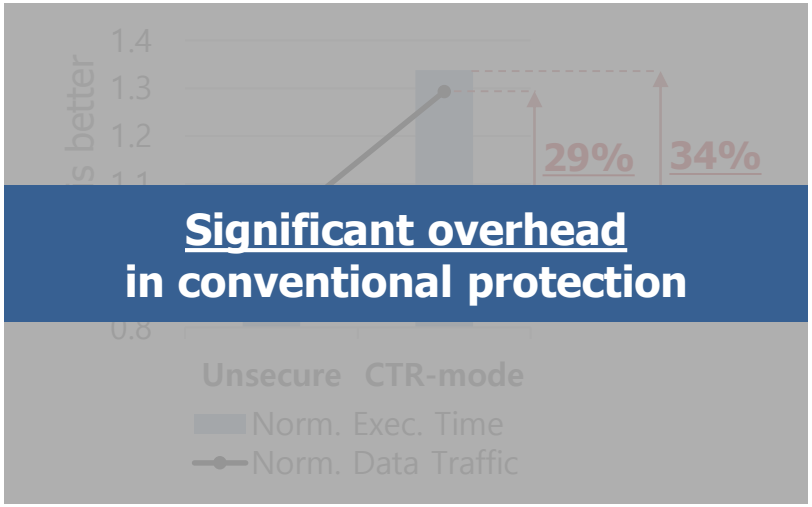



**Conventional 64B-granular Protection**




**Prior Domain-specific Memory Protection**

1. Common Counters [1]
2. Dual-MAC [2]

[1] Common Counters: Compressed Encryption Counters for Secure GPU Memory (HPCA 2021)
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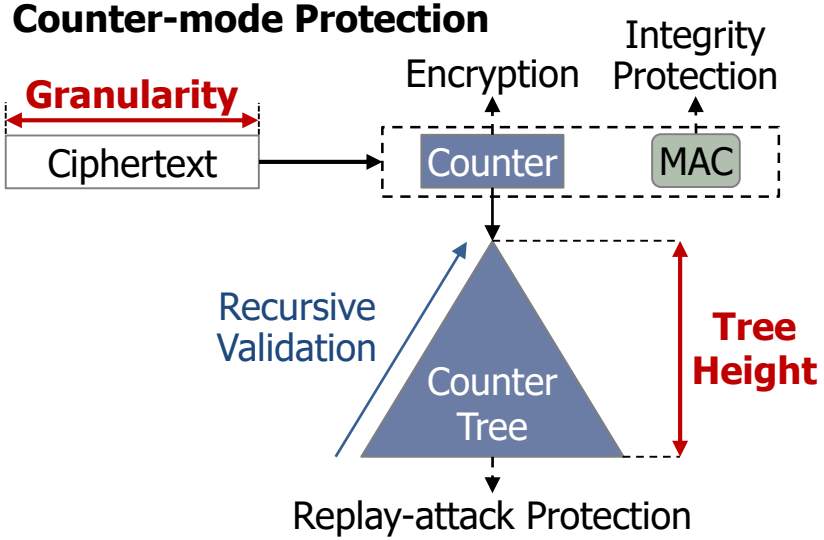
# Prior Memory Protection Schemes

**Counter-mode Protection**

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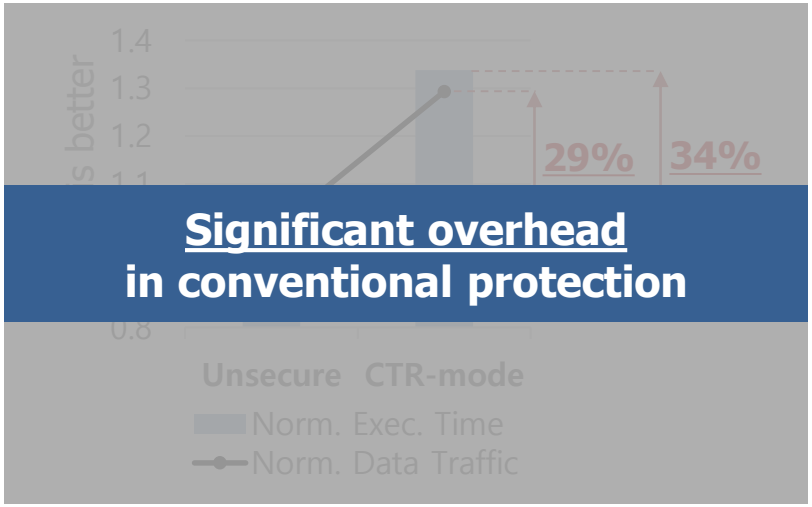


**Prior Domain-specific Memory Protection**

1. Common Counters [1]
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3. Software-managed Granularity [3-4]

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[3] MGX: Near-zero Overhead Memory Protection for Data-intensive Accelerators (ISCA 2022)
[4] GuardNN: Secure Accelerator Architecture for Privacy-preserving Deep Learning (DAC 2022)

# Prior Memory Protection Schemes

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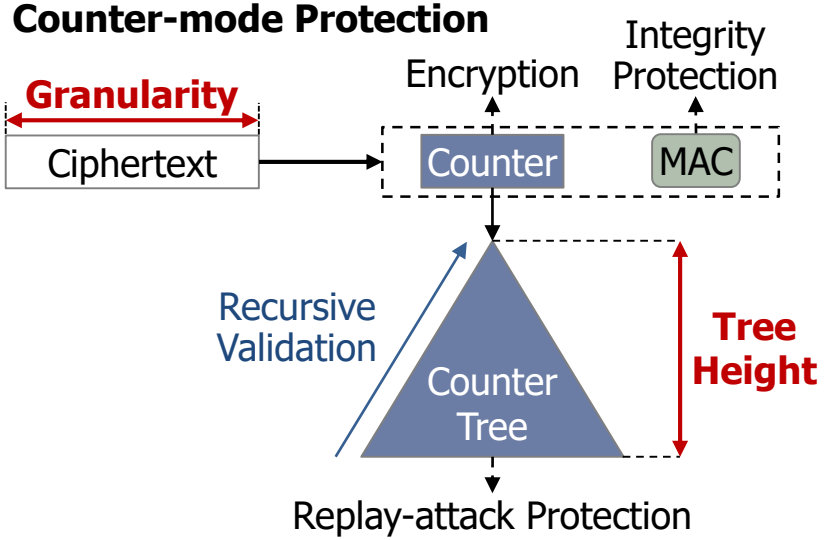


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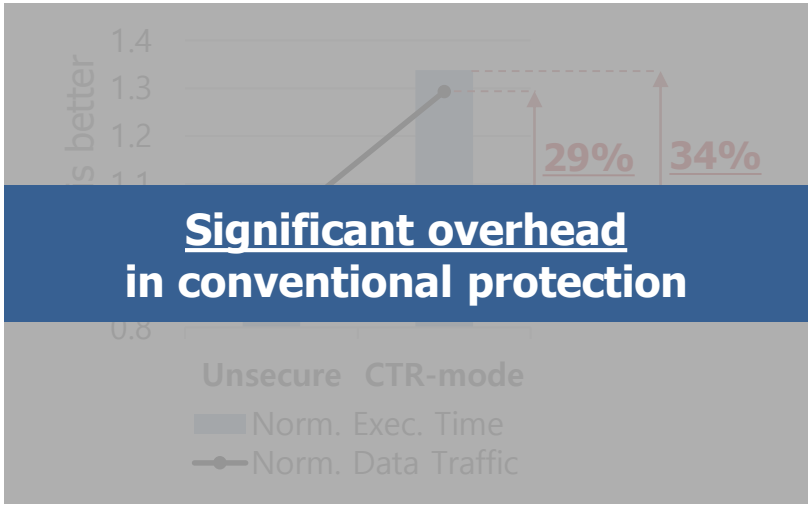


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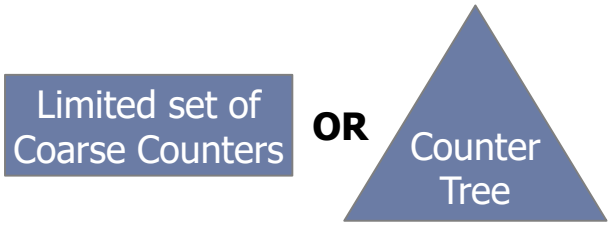


2. Dual-MAC [2]

3. Software-managed Granularity [3-4]


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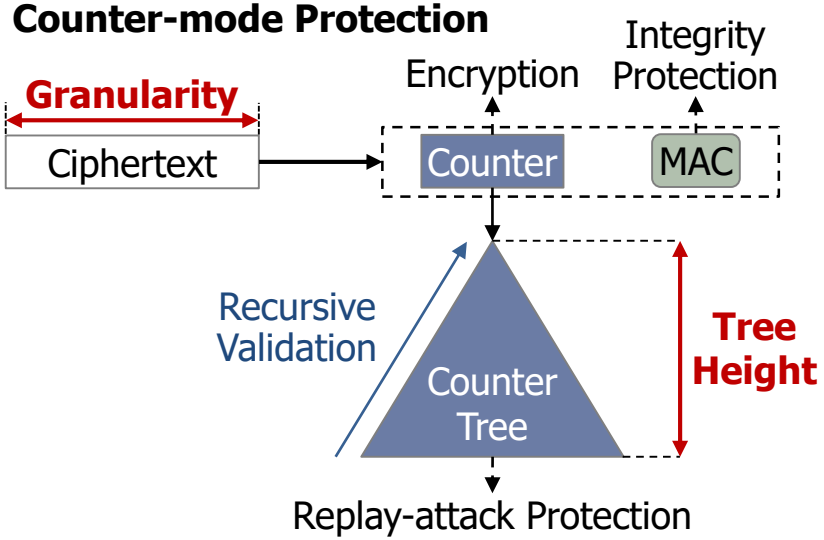


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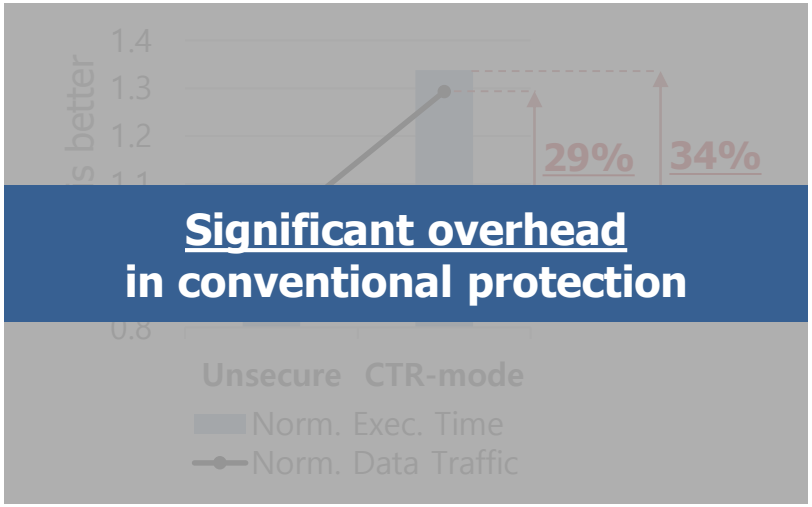


**Prior Domain-specific Memory Protection**

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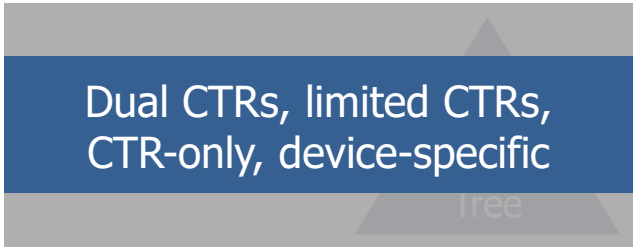


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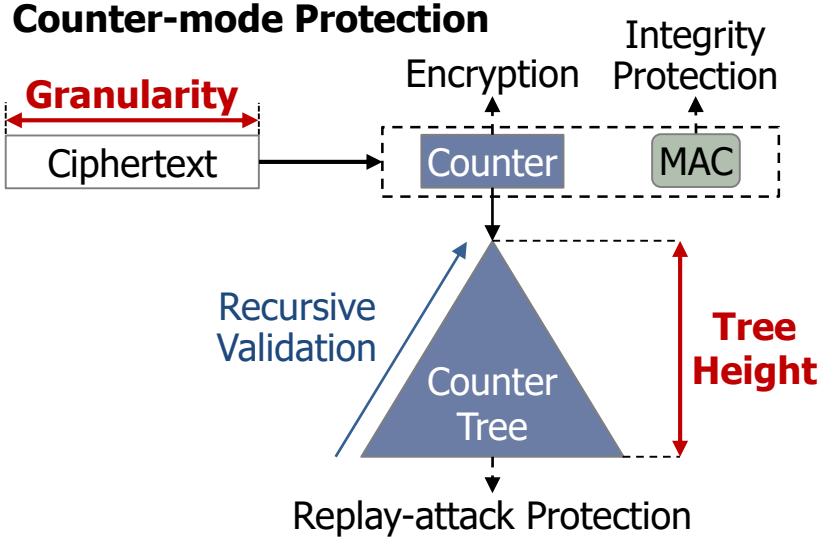
Temp

# Prior Memory Protection Schemes

**Counter-mode Protection**

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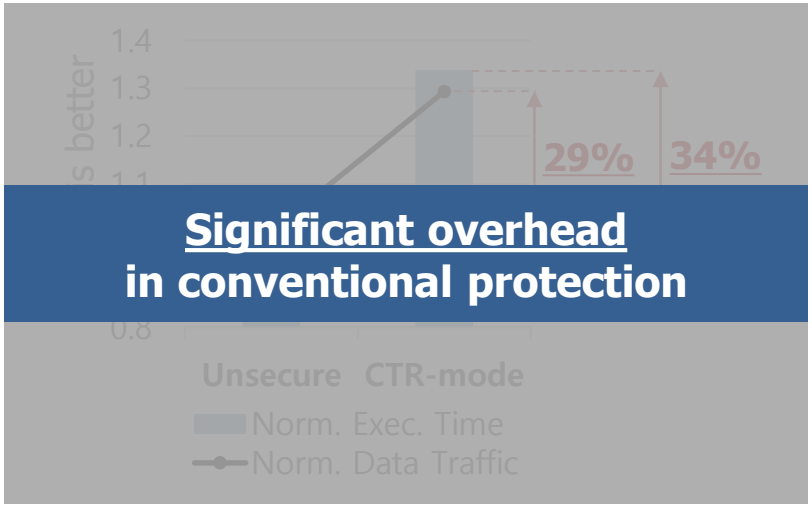


**Prior Domain-specific Memory Protection**

1. Common Counters [1]

Dual CTRs, limited CTRs, CTR-only, device-specific

2. Dual-MAC [2]

Coarse MAC

**OR**

Fine MAC

3. Software-managed Granularity [3-4]

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Temp

# Prior Memory Protection Schemes

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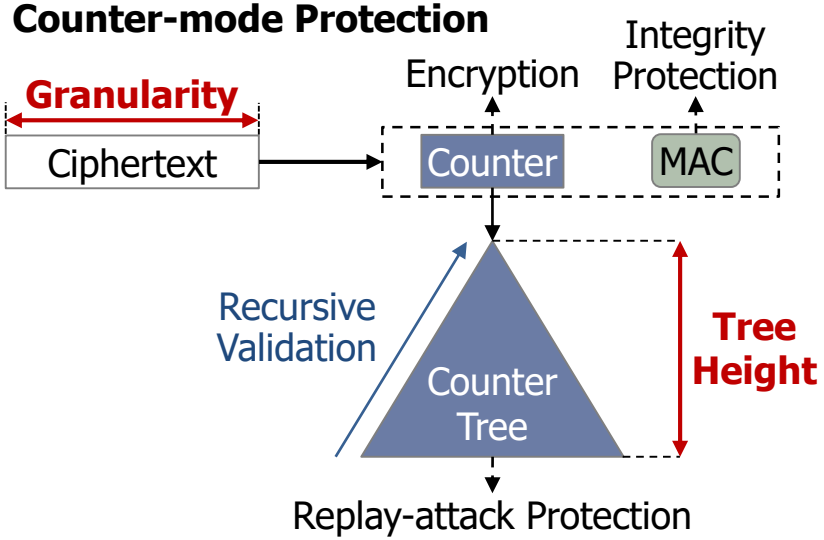


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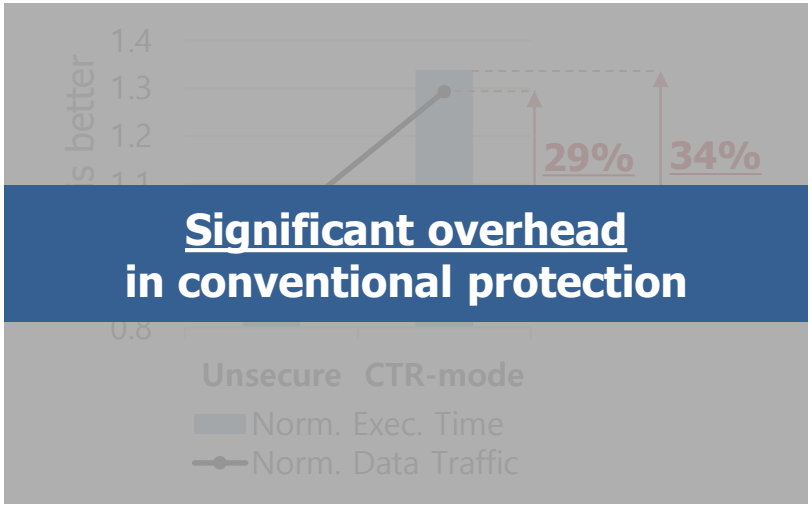


**Prior Domain-specific Memory Protection**

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Dual MACs, MAC-only

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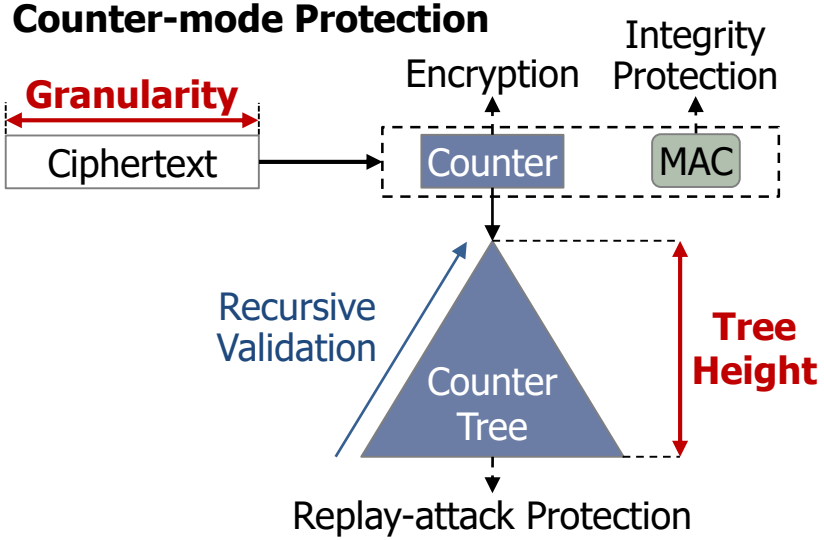
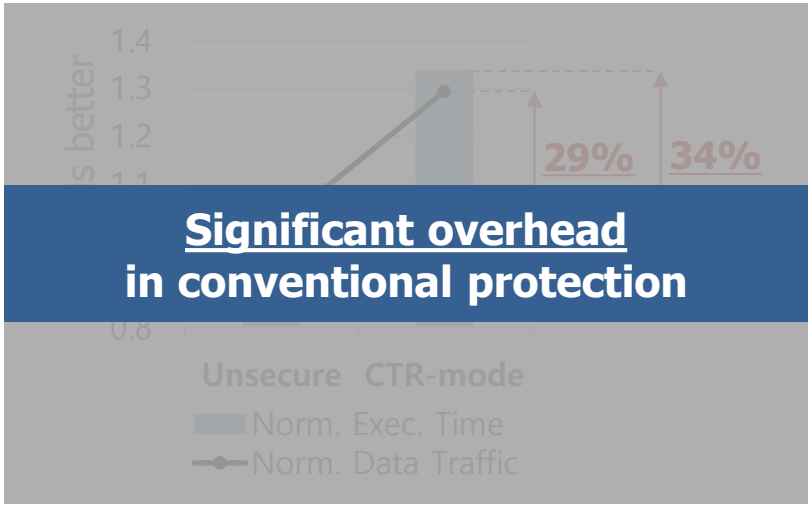
# Prior Memory Protection Schemes

### Counter-mode Protection




### Conventional 64B-granular Protection




### Prior Domain-specific Memory Protection

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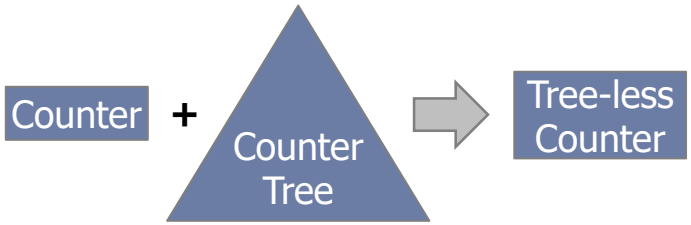
2. Dual-MAC [2]

Dual MACs, MAC-only

3. Software-managed Granularity [3-4]

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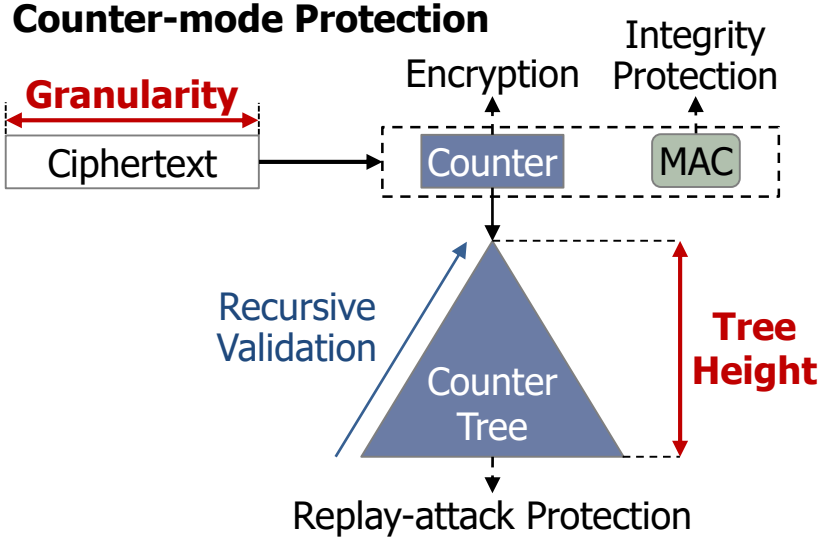


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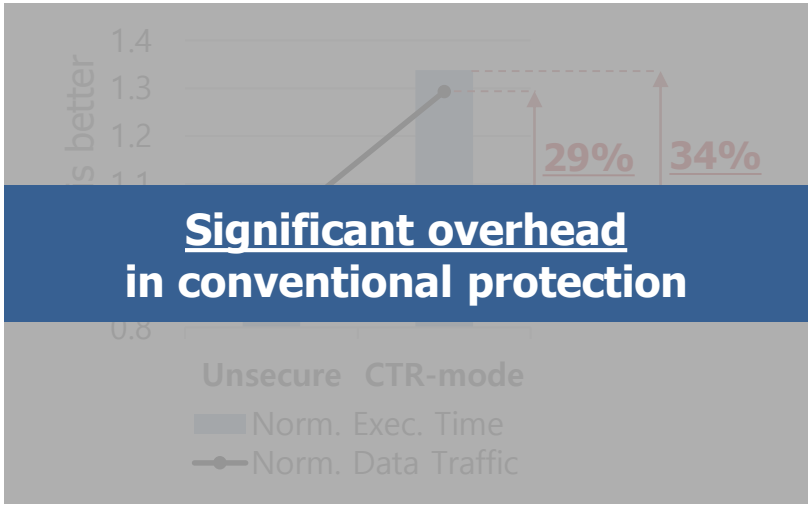


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2. Dual-MAC [2]

Dual MACs, MAC-only

3. Software-managed Granularity [3-4]

Application-specific, device-specific

[1] Common Counters: Compressed Encryption Counters for Secure GPU Memory (HPCA 2021)
[2] Adaptive Security Support for Heterogeneous Memory on GPUs (HPCA 2022)
[3] MGX: Near-zero Overhead Memory Protection for Data-intensive Accelerators (ISCA 2022)
[4] GuardNN: Secure Accelerator Architecture for Privacy-preserving Deep Learning (DAC 2022)

Temp